A Multiparameter Implantable Microstimulator SOC

Chua-Chin Wang, Tzung-Je Lee, Yu-Tzu Hsiao, U Fat Chio, Chi-Chun Huang, Jia-Jin J. Chin, and Ya-Hsin Hsueh

***Abstract*—Various implantable microstimulators have been proposed for clinical applications in recent years. Most of the no-battery implanted devices can be powered by a transcutaneous magnetic coupling, which basically utilizes an external transmitter coil to power and communicate with the implanted device. Small chip area and low power consumption are the keys of the implanted device. Therefore, we propose a C-less (no capacitor) area-saving ASK demodulator in this work to get rid of those large discrete capacitors required for low-frequency ASK demodulation. Additionally, a power regulator supplying a stable VDD_OUT is also built in to resolve the unstable supply voltage problem resulted from the inductive link. Besides, a multiparameter control protocol which has an area advantage over microcontroller-based solutions is also proposed for various pain treatments of muscles and stimulating applications.**

***Index Terms*—Implantable, microstimulator, neural interface, non-return-to-zero (NRZ), system-on-chip, telemetry.**

I. Introduction

With the use of deeply miniaturized silicon technologies, the implantable microelectrical stimulator has become an astonishing therapeutic tools. The implantable microelectrical stimulators and the entire system are widely used in the treatment of the bladder leakage control [1], interrupt of pains, muscle nerve stimulation [2], and cochlear implants [3]. The stimulus frequency, current, and waveform of each application are different. Usually, it needs a frequency of 20–200 Hz, a duration of 0.21–1.4 ms, and a current of 11 mA or more to cover denervated muscle, pain treatment, bladder stimulation, and sacral nerve stimulation [4]–[7].

There are two major types of implantable device designs. The first type employs microcontrollers [8]. It has a better flexibility to change different functions by programming, but the size is extremely large. The second type is based on deep-submicron silicon semiconductor technology, which must follow certain design requirements to fabrication. The chip size, by contrast, is very small, possibly only 1–3 mm^2, and is very suitable for implantable microstimulators [9]–[11]. The critical drawback of this kind of chip is lack of flexibility for various applications. We, thus, propose a multiparameter implantable SOC which utilizes many parameters encapsulated in transmitted packets to resolve this problem. There are a total of seven parameters in the protocol proposed in this paper. They are all controllable by an external device to provide most of the currently required medical stimulations.

II. Multiparameter Neural Interface Microstimulator System

The infrastructure of the entire microstimulator system is given in Fig. 1. The transmitted RF electromagnetic wave is picked up by a receiver coil of the implanted device, and the electromagnetic energy is transferred into regulators serving for the implanted chip. Meanwhile, the transmitted data modulated in RF signal is demodulated and decoded to determine stimulation patterns and channel selections.

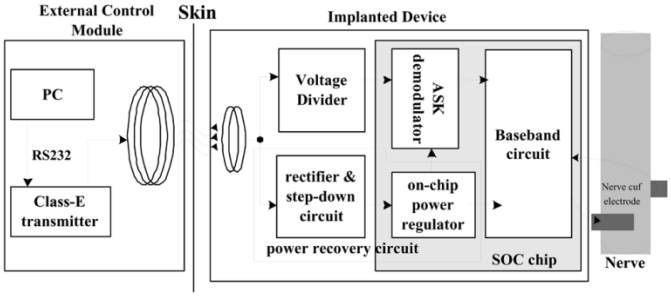

Fig. 1. Wireless neural stimulating system.

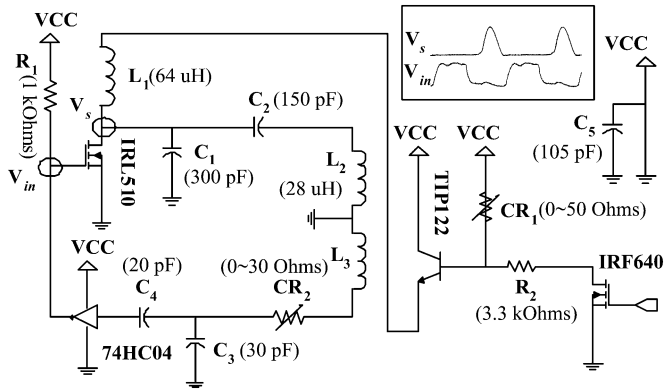

Fig. 2. Schematic diagram of the Class-E amplifier.

In order to supply enough power for this low coupling application, a Class-E amplifier with ASK modulation is used. The carrier frequency is chosen to be 2 MHz, which possesses an adequate transmission rate and minimal tissue absorption [12]. Fig. 2 shows the schematic of the Class-E amplifier. It uses a feedback circuit (L_3, CR_2, C_3, C_4, and 74HC04) to achieve self-oscillating [13]. Notably, V_{in} and V_s have a phase difference of 180 degrees to avoid the power dissipation from the MOS IRL510. The transmitter operates with a 5-V supply, consumes 0.6 A, and oscillates at a frequency of 2 MHz. The transmission range is measured to be 1.5 cm from the center of the transmitter coil.

Fig. 3 shows the schematic of the receiver RF front-end. The outputs DATA and V_power are sent to the ASK demodulator and regulators, respectively. The tuning capacitor CR1 adjusts the resonance frequency of the receiver. The rectified voltage is stored in the first storage capacitor CR2. The resistor RR1 and the Zener diode DR5 provide a bias voltage for the step-down circuit.

III. SOC Design of the Multiparameter Neural Interface Microstimulator

A. System Design

1) Power and the Regulator: The power of the core circuit on the chip is generated by the induced RF signal. On-chip power regulators [14] are required to supply stable output voltages VDD_OUT to the internal circuit by regulating the power V_power (VDD_IN) coming from the step-down circuit. There are a total of four regulators in this SOC chip, including one for I/O pads, one for ASK demodulator, and

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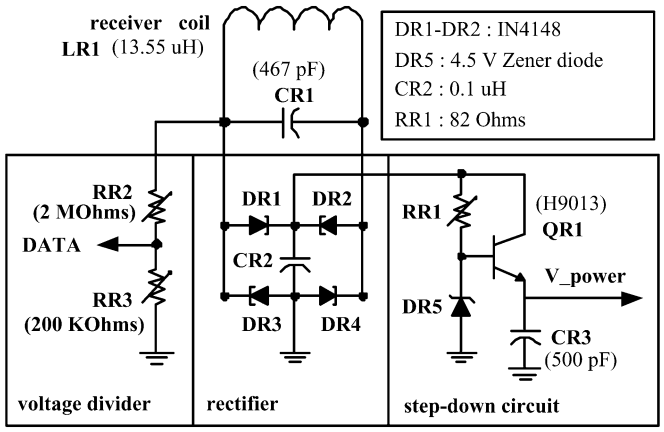

Fig. 3. Schematic of the receiver RF front-end.

TABLE I
SYSTEM PROTOCOL

packet1	0	1	0	1	0	1	0	1	0	1
packet2	0	1	0	1	0	1	0	1	0	1
packet3	0	1	0	1	0	1	0	0	1	1
DATA1_1	0	AD		P	MAG					1
DATA1_2	0	CONT	DUR		INTV			WAVE	PAR	1
...	...									
END	0	0	0	0	0	0	0	0	0	0

TABLE II
SPECIFICATION OF STIMULATION DURATION AND INTERVAL TIME

DUR	00	01	10	11				
dur (ms)	0.1	0.5	1	2				
INTV	000	001	010	011	100	101	110	111
intv (ms)	0	0.1	0.2	1	3	5	10	50

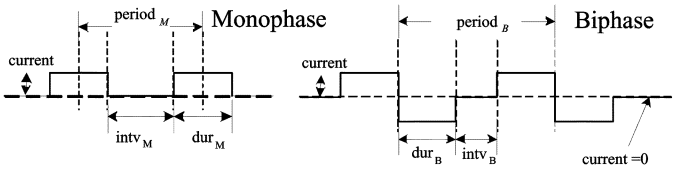

Fig. 4. Definition of duration and interval.

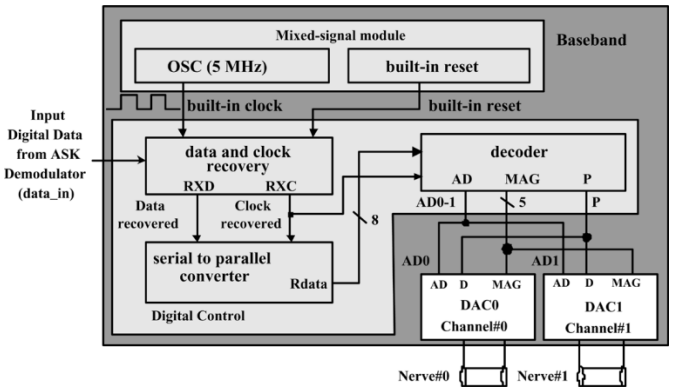

Fig. 5. Baseband architecture of the implantable device.

two for the baseband module (digital blocks) and stimulator circuits (analog blocks).

2) On-Chip C-Less ASK Demodulator: The ASK demodulator is divided into four parts: 1) half-wave rectifier; 2) envelope detector; 3) threshold detector; and 4) load driver [14], where a two-stage operational amplifier (OPA) acts as an unit gain buffer to resist the negative voltage. Thus, it is basically a half-wave rectifier.

3) Packet Format: The data packet format follows the RS232 standard because of a limited bandwidth. The valid packets of the system protocol are listed in Table I and discussed in the following description. (The first bit is the RS232 start bit and the last "1" bit is the end bit of RS232 standard.)

1) Synchronization: The packets 1–2 are used to synchronize the external and internal clocks.
2) Start: The packet 3 is a start packet, which triggers the stimulating function.
3) Data packets (DATA1_1–DATA1_2...): All of the stimulation control parameters are encoded in these packets.

   DATA1_1: The second and third bits (AD) are the address bits selecting which one or both of the two channels are enabled and excited. The fourth bit (P) determines the polarity (positive or negative) of the output stimulating current. The magnitude field is composed of 5 bits (MAG) which denote the magnitude of the stimulating current.

   DATA1_2: The second bit (CONT) is the continuous mode selection. The microstimulator keeps the stimulation pattern the same when the command in the continuous mode is given. Hence, the external device only needs to transfer the power without the necessity of encoding data. The third and fourth bits (DUR) and the fifth through seventh bits (INTV) are the duration and interval of the stimulation pulse, respectively. The detailed specification is given in Table II. The eighth bit (WAVE) selects the stimulation waveform to be monophase or biphase. The ninth bit is the parity check bit (PAR) of all data packets to avoid any erroneous stimulation. The received data are ignored when its validity is not confirmed.

$$\mathrm{Freq}_{\mathrm{mono}} = 1/\mathrm{period}_M = 1/\mathrm{dur}_M + \mathrm{intv}_M$$

and

$$\mathrm{Freq}_{bi} = 1/\mathrm{period}_B = 1/2 \cdot \mathrm{dur}_B + \mathrm{intv}_B$$

are the frequency equations of monophasic and biphasic waveforms, respectively, where the definitions of $\mathrm{duration}_i$ and $\mathrm{interval}_i$, $i = B, M$, are shown in Fig. 4.

4) END: The END packet means this stimulation is finished.

4) Baseband Schematic Design: Referring to Fig. 5, the internal architecture of the implantable SOC chip is revealed. Initially, VDD_OUT rises from the ground voltage. The built-in clock starts oscillating. Then, the built-in reset signal (the rising edge) resets the digital baseband circuit. The finite state machine (FSM) of the entire flow is shown in Fig. 6.

5) Data and Clock Recovery: When the synchronization packets are received, the clock recovery circuit counts the number of cycles of the 5-MHz built-in clock during each positive edge and negative edge of the synchronization packets. The cycle numbers are recorded and then used to generate the system clock. Then, the data can be recovered.

6) Serial to Parallel Converter: The recovered packet is converted into a parallel format by the serial-to-parallel converter.

7) Decoder: The decoder receives the recovered clock and the parallel data. Then, it sends AD (address), MAG (magnitude), and P (polarity) signals to the digital-to-analog converter (DAC) to determine which channels are to be excited, the strength and the direction of the stimulus current, respectively. As soon as the END packet is received, the stimulation stops.

8) DAC: The DACs directly supply driving currents to their associative nerves to serve as a stimulus. The magnitude of the current is

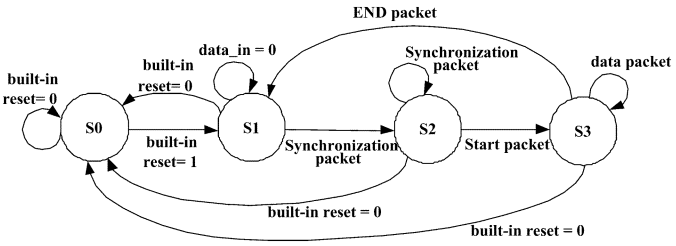

Fig. 6. State transition of the system's FSM.

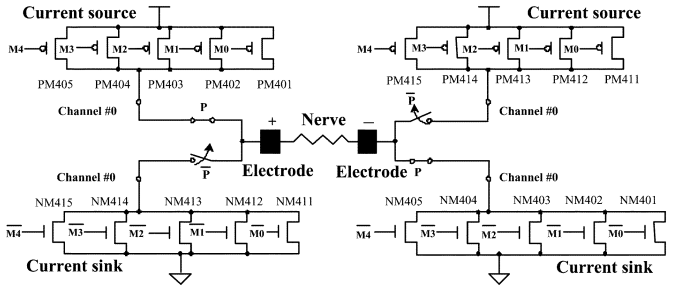

Fig. 7. Interface of DAC and the nerve.

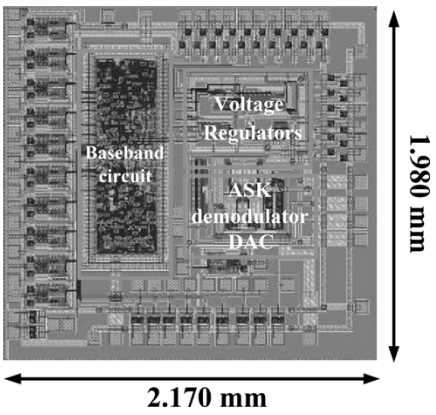

Fig. 8. Die photograph of the proposed design.

determined by the MAG field of the data packets through the five signals, denoted by M4, M3, M2, M1, M0 in Fig. 7. The aspect ratio (W/L) for MOSs (in Fig. 7) XM4Y5, XM4Y4, XM4Y3, XM4Y2, XM4Y1 is 16, 8, 4, 2, 1, respectively, produces a binary-weighted stimulating current, where $X = N, P$ and $Y = 0, 1$. Thus, a 32-level stimulus current is obtained by the summation of the currents via the mentioned MOSs. The polarity signal (P) from the decoder is used to control the switches to select the current direction. When P is high, the current flows from the positive node to the negative node, and *vice versa*. When $AD = 0$, the switches in the DAC for nerve #0 are closed, as shown in Fig. 7. Thus, the stimulus for nerve #0 is activated.

IV. Simulation and Measurement

The chip is designed by using TSMC 0.35-μm two-poly four-metal (2P4M) CMOS process. The die photograph is shown in Fig. 8. Fig. 9 shows the measured result of the proposed microstimulator. The system clock is recovered after the synchronous package is received. The channels #0 and #1 are selected to supply their maximum stimulus current in the continuous mode. Thus, the stimuli continue until the next command is received. The channel #0 is selected to generate the maximal magnitude (1.75 mA at 1-kΩ load) stimulating current.

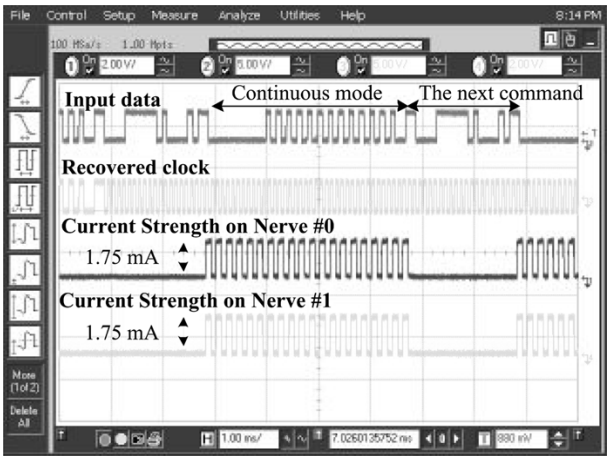

Fig. 9. Measured result of the proposed SOC chip.

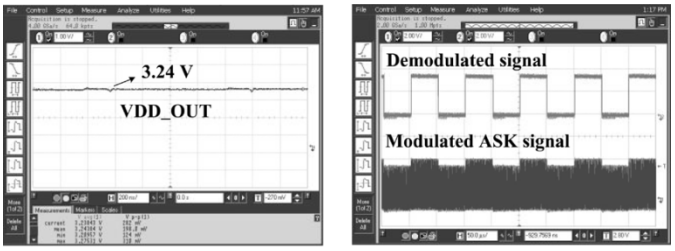

Fig. 10. (a) Measured output voltage of the regulator (25 °C, 4.4–5.5-V input). (b) Measured result of ASK demodulator.

TABLE III
Measured Characteristics of the Regulator and ASK Demodulator

input voltage of regulator	4.4∼5.5 V, 0∼2 MHz
output voltage of regulator	3.24 V±6.11% (36∼41^{o}C)
freq. of the input	data rate / carrier freq.: 10 Kbps / 2 MHz
voltage level of the input	logic low / high level: 2.9 V / 3.5 V
freq. of the output	20 KHz / duty cycle: 47.5%
logic level of the output	logic low / high level: 0.3 V / 3.24 V
core area	0.0511 mm^2
Note : the load at the O/P of ASK demodulator is 10pF and 1KΩ.	

Fig. 10(a) shows the measurement of the regulator. The voltage VDD_OUT is 3.24 V coupling a maximum ripple of 198 mV despite the severe varying VDD_IN. Thus, VDD_OUT is stabilized by the regulator. The measurement of the modulated and the demodulated signal is shown in Fig. 10(b). Notably, the negative voltage of the input modulated ASK signal is clamped by the electrostatic discharge (ESD) protection circuit in the input pad. The measurement characteristics of the voltage regulator and the ASK demodulator are given in Table III.

V. Conclusion

An SOC-based solution for implantable neural interfacing design for treatment of pain in muscles is presented. The small-area solutions for an ASK demodulator and a stable 3.24-V on-chip voltage regulator design are also presented in this paper. The proposed design is intended to support the same flexibility of traditional electrical stimulators in the implantable device and minimize the size at the same time. It can also support several parameters for different usages in muscle electrical stimulation applications. The comparison of the proposed design with several prior works is summarized in Table IV. Our design possesses

TABLE IV
COMPARISON WITH PRIOR WORKS

	[9] (1997)	[10] (1997)	[11] (1999)	ours
Technology	CMOS 1.2 μm	Bi-CMOS 3 μm	Bi-CMOS 3 μm	CMOS 0.35 μm
size (mm^2)	16×2	1.36×7.5	2.0×8.7	2.17×1.98
No. of channels	4 (bipolar)	1	8	2 (bipolar)
Parameter #	5	2	5	7
Regulated voltage(V)	N/A	4.5 and 9	4	3.24
Carrier Freq. (Hz)	AM at 20M	AM at 2M	ASK at 4M	ASK at 2M
Data rate (bps)	300K	N/A	8.3K	10K
Stim. freq. (Hz)	2∼1500	1∼40	$\leq$170	20∼10K
Duration of stim. (μs)	10∼2550	10∼200	4∼2025	100∼2000
Output current (mA)	0∼6.3	10	0∼2	0∼1.8
Power (mW)	N/A	45∼55	15	80 (average),¶ 120 (max.)¶

¶: these terms include the pad's power consumption

the edge regarding parameter numbers, chip size, and core power consumption. In the future, the SOC chip will not only carry out the electrical stimulations, it will also be able to exchange electrical signals between human nerves and an external electronic control device.

REFERENCES

[1] J. S. Walter, J. S. Wheeler, W. Cai, W. W. King, and R. D. Wurster, "Evaluation of a suture electrode for direct bladder stimulation in a lower motor neuron lesioned animal mode," *IEEE Trans. Rehabil. Eng.*, vol. 7, no. 2, pp. 159–166, Jun. 1999.

[2] G. E. Loeb, F. J. R. Richmond, D. Olney, T. Cameron, A. C. Dupont, K. Kood, R. A. Peck, P. R. Troyk, and H. Schulman, "BION™ bionic neurons for functional and therapeutic electrical stimulation," in *Proc. 20th Annu. Int. Conf. IEEE Engineering in Medicine and Biology Soc.*, vol. 5, Nov. 1998, pp. 2305–2309.

[3] R. E. Isaacs, D. J. Weber, and A. B. Schwartz, "Work toward real-time control of a cortical neural prosthesis," *IEEE Trans. Rehabil. Eng.*, vol. 8, no. 2, pp. 196–198, Jun. 2000.

[4] T. Eken and K. Gundersen, "Electrical stimulation resembling normal motor-unit activity: Effects on denervated fast and slow rat muscles," *J. Physiol.*, vol. 402, no. 1, pp. 651–669, Aug. 1988.

[5] C. Bohotin, M. Scholsem, S. Multon, D. Martin, V. Bohotin, and J. Schoenen, "Vagus nerve stimulation in awake rats reduces formalin-induced nociceptive behavior and fos-immunoreactivity in trigeminal nucleus caudalis," *J. Pain*, vol. 101, no. 1–2, pp. 3–12, Jan. 2003.

[6] C. H. Seif, P. M. Braun, S. Bross, J. Scheepe, J. Weiss, S. Schumacher, S. Zendler, P. Alken, and K. P. Junemann, "Selective block of urethral sphincter contraction using a modified brindley electrode in sacral anterior root stimulation of the dog," *Neurourol. Urodyn.*, vol. 21, no. 5, pp. 502–10, 2002.

[7] E. Ganio, A. R. Luc, G. Clerico, and M. Trompetto, "Sacral nerve stimulation for treatment of fecal incontinence: A novel approach for intractable fecal incontinence," *Dis. Colon Rectum*, vol. 44, no. 5, pp. 619–629, May 2001.

[8] S. Salmons, G. T. Gunning, I. Taylor, S. R. Grainger, D. J. Hitchings, J. Blackhurst, and J. C. Jarvis, "Implantable stimulators based on semi-custom CMOS technology or low-power microcontroller architecture," *Med. Eng. Phys.*, vol. 23, no. 1, pp. 37–43, Jan. 2001.

[9] K. Arabi and M. A. Sawan, "Electronic design of a multichannel programmable implant for neuromuscular electrical stimulation," *IEEE Trans. Rehabil. Eng.*, vol. 7, no. 2, pp. 204–214, Jun. 1997.

[10] B. Ziaie, M. D. Nardin, A. R. Coghlan, and K. Najafi, "A single-channel implantable microstimulator for functional neuromuscular stimulation," *IEEE Trans. Biomed. Eng.*, vol. 44, no. 10, pp. 909–920, Oct. 1997.

[11] J. A. V. Arx and K. Najafi, "A wireless single-chip telemetry-powered neural stimulation system," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 1999, pp. 214–215.

[12] J. C. Lin, "Computer methods for field intensity predictions," in *CRC Handbook of Biological Effects of Electromagnetic Fields*, C. Polk and E. Postow, Eds. Boca Raton, FL: CRC Press, 1986, ch. 2, pp. 273–313.

[13] C. M. Zierhofer and E. S. Hochmair, "High-efficiency coupling-insensitive transcutaneous power and data transmission via an inductive link," *IEEE Trans. Biomed. Eng.*, vol. 37, no. 7, pp. 716–722, Jul. 1990.

[14] C.-C. Wang, Y.-H. Hsueh, U. F. Chio, and Y.-T. Hsiao, "A C-less ASK demodulator for implantable neural interface chips," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, vol. 4, May 2004, pp. 57–60.