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BASEBAND DESIGN OF A WIRELESS TRANSCEIVER FOR IMPLANTABLE NEURAL INTERFACE

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ABSTRACT

An implantable SOC-based neural interfacing baseband design including controllable stimulators and telemetry for data and power transmission is proposed. The micro-stimulator consists of multi-channel addressable current-source stimulators. The implanted device can be powered by transcutaneous magnetic coupling, using an external transmitter coil to power and communicate with implanted devices. It can avoid the risk of causing infection and the problem of limited battery life. The SOC-based implantable system will be compatible with several prior neuronics assemblies. The neural interface SOC implementation is aimed at the control and monitor of the neural-interfaces which might be applied to the area of neural prosthetics or orthotics replacing or restoring functions lost due to damage to the nerve system.

Key words: implantable, neural interface, SOC, wireless, DAC

I. INTRODUCTION

Traditional medical treatment has been drastically influenced by the advance of modern science and technology. One of the astonishing medicate tools is the implantable micro-electrical stimulators thanks to the deeply miniaturized silicon technology. The implantable micro-electrical stimulators as well as the entire system are widely used in the treatment of the bladder leakage control [11], interruption of pains, the shaking syndromes of Parkinson's disease, muscle nerve stimulation, and Cochlear implants [4].

The electrical stimulator techniques are expected to be heavily used in the nerve systems where the electronic signals may be invoked to connect broken nerves, i.e., neural prostheses. The proposed design is intensively focused on an SOC-based system which leads to the restoration of functional movements of paralyzed extremities, e.g., paraplegia, quadriplegia, etc. Both the stimulative and sensory functions, therefore, have to be considered simultaneously. Paralysis patients might have chances to re-gain the sensing capability by the transmission of these electronic signals between their brain and muscle nerves. The proposed implantable SOC-based baseband design includes controllable constant-current stimulators, and telemetry for data and power transmission. The micro-stimulator consists of multi-channel addressable current-source stimulators. The implanted device can be powered by transcutaneous magnetic coupling, using an external transmitter coil to power and communicate with implanted devices. It can avoid the risk of causing infection and the problem of limited battery life. The SOC-based implantable system will be compatible with several prior neuronics assemblies, including multi-shank probes [9], PEAs (planar electrode array) [5], regeneration-typed microelectrodes [6], and particularly injected micromodular BIONs (BIOnic Neurons) stimulators [7]. Besides the SOC design methodology which is required to carry out the core chip, both the micro-electronic packaging method (e.g, SMT, SiP and flip-chip packaging) and the bio-compatible materials (e.g, polyimide, or hermetic capsule) [5] are needed to fabricate the final prototype of the implantable SOC-based device. Thanks to the highly advanced semiconductor process and IC design, the size of the implanted SOC device is expected to be far smaller than that of all of the prior electrical stimulators, including capsuled BIONs, cardiac pacemakers, and cochlear implants.

II. BASEBAND DESIGN OF A WIRELESS NEURAL INTERFACE

We propose an SOC (system-on-chip) chip to carry out the mission utilizing wireless and non-penetrating

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transmission to accept external instructions and execute the required stimulations. The entire electrical micro-stimulus system is given in Fig. 1.

2.1 System design

Power: Due to the demand of the small-sized receiver coil of the implanted device, the power transmission efficiency in the micro-devices is quite low. In order to supply enough power to the implanted device, a high efficiency transmitter/amplifier must be used. Class-E power amplifiers show efficiency above 90% and are suitable for such a low coupling application. Hence, the power amplification is based on the class-E amplifier and self-oscillating. The coupling of the coil influences the oscillation frequency. The resulting operation frequency offset yields an improved power transmission performance, since the oscillation frequency tracks the absolute transmission efficiency maximum. Fig. 2 and 3, respectively, show the class-E amplifier and the measured output waveforms.

Regulator: An on-chip power regulator is required to supply a stable VDD voltage to the internal digital core by regulating the power supplied by the on-chip coupling coil. Large batteries, thus, are not needed in such a system. The implanted device design must be aimed at reducing the circuit area and power. Hence, the number of passive elements must be minimized. The LDO (low dropout) voltage regulator circuit, as shown in Fig. 4, is composed of 3 sub-circuits: a bandgap bias, an error amplifier, and a pass element [12], [13], [14]. The one-stage high-gain differential amplifier increases the operation bandwidth, lock time, and the PSRR (power supply rejection ratio). When the aspect ratio of the pass element PM211 increases, not only does it decreases the dropout voltage, but also increases the driving capability.

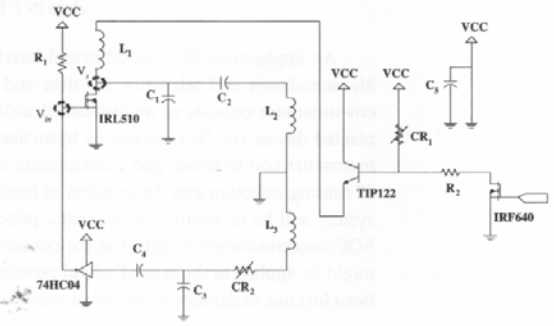

Fig. 2 Schematic diagram of the Class-E amplifier.

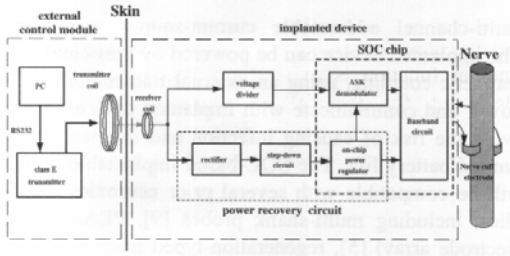

Fig. 1 Wireless neural stimulating system.

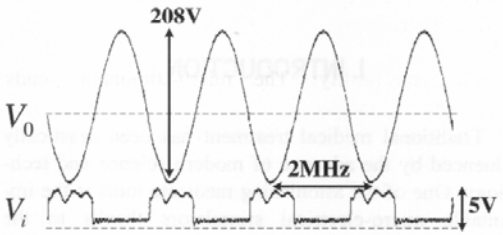

Fig. 3 Measurement result of the class-E amplifier.

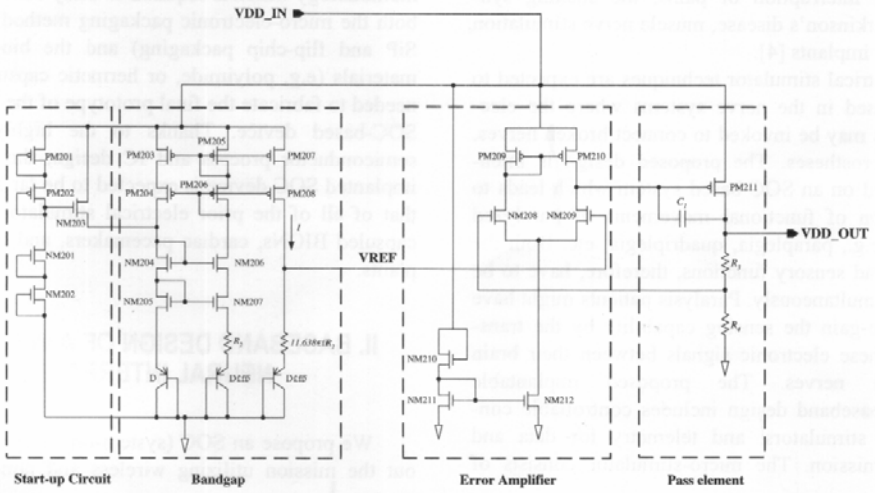

Fig. 4 Schematic diagram of the power regulator.

Safety: Since the SOC is targeted to be an implantable device, safety is naturally our primary concern. Manchester code is used for noise rejection reasons in the digital wireless communication [15].

Packet Format: The format of a valid packet is shown in Fig. 6. The first field composed of 5 bits is the START field. Five consecutive zero's trigger the stimulating function. The ADDRESS field comprises 3 bits to select which of the three channels are enabled and excited. The D bit determines the direction of the stimulating current. In other words, it is the sign of the current. The final MAG field is the amplitude of the stimulating current. These 5 bits are fed to the DAC associated with each channel.

RF Band Selection: Regarding the choice of carrier frequency band, we must consider that the electromagnetic wave absorbed by the tissue of the body is proportional to the frequency of the electromagnetic waves. Besides, lower carrier frequencies will influence the transmission data rate. Thus, the general carrier frequency of an implanted system is within ISM band, e.g., 1 to 20 MHz. Because of the absorption of biological tissue and the interruption to other medical instruments, the 2 MHz carrier frequency is chosen in our study [7].

Digital Modulation Scheme: The scheme in the data transmission comprises data coding and modulation. In order to reduce the size of the implanted circuit, amplitude-shift keying (ASK) modulation is used in this device.

Bio-compatibility: The micro-stimulator sends electrical pulses through the cuff electrodes to the nerve trunks as shown in Fig. 1. The magnitude, as well as the pulse width required by neural trunks are given in Table 1 based on [1], [2], [3], [8], and [10]. The nerve is deemed as a 1 KΩ resistive load instead of a capacitive load, since the stimulus current is absorbed. In short, the strength of stimulus applied to a nerve can be controlled by an external device through the wireless transmission.

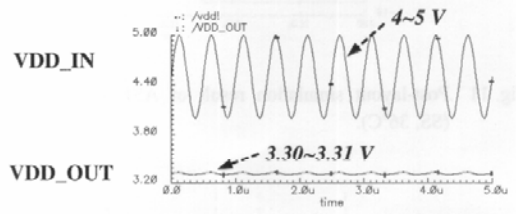

Fig. 5 Post-layout simulation result of power regulator (SS, 36°C)

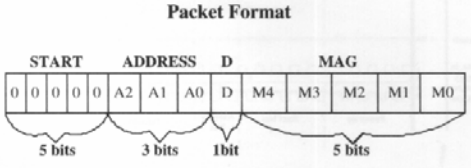

Fig. 6 Packet format of data transmission.

2.2 Schematic design

The architecture of the implantable SOC chip has been revealed in Fig. 1. The external control circuit is a PC-based interface to generate the command packets. The external parts of the system are described as follows.

Class E transmitter: Fig. 2 is the circuit design of the Class-E amplifier. It switches the serial-parallel LC resonant circuit to induce the high resonant AC voltage and current through the transmitter coil. The circuit is operated between series and parallel resonant networks via a switch (IRL510). Such resonant networks consist of capacitor C_1, C_2, and transmitter coil L_2.

The ASK signal is coupled to the Class-E by the circuit composed of IRF640, TIP122, CR_1, R_2, and L_1. The combination of the DC supply and the RF-choke (L_1) acts as a current source charging the resonant network and creating a transient voltage across the switch. The Class-E amplifier uses a feedback circuit consisting of L_3, CR_2, C_3, C_4, and 74HC04, to achieve self-oscillating.

Referring to Fig. 7, the internal architecture of the implantable SOC chip is revealed. OSC is a ring-based 5 MHz clock generator, while the "BIST & Reset" comprises the initialization and test settings of the system. The rest of the chip are described as follows.

Manchester Decoder: It receives the bit stream, Data_in, generated by the ASK demodulator (not shown) and executes the framing of valid packets, i.e., Data_out. Another function is to recover a 10 KHz clock, i.e. Clock_out for the following FSM and S/P (serial-to-parallel) converter.

FSM (finite state machine): There are a total of 4 states to execute the required stimulating functions as shown in Fig. 8.

Table 1 Bio-compatible requirements of electrical pulse

	stimulating	blocking
freq.	10 - 100 Hz	1 - 2 KHz
current	1 - 3 mA	1 - 3 mA
pulse width	100 - 1000 μs	30 - 300 μs

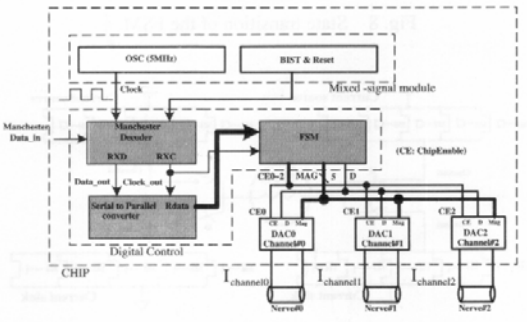

Fig. 7 Baseband architecture of the implantable device.

S0: When the decoded bit stream consists of consecutive 1's, the system simply pumps the voltage supplied by the built-in regulator in the BIST module. As soon as any 0 is detected, FSM moves into S1.

S1: If five consecutive 0's are detected, FSM moves into S2. Otherwise, it reverts back to S0.

S2: This state decodes the ADDRESS field : A_2, A_1, and A_0, respectively, to enable DAC_2, DAC_1, and DAC_0 if the corresponding bit is set.

S3: The D bit determines the current direction of the enabled DAC's. The amplitude of the stimulating current is controlled by M_4, …, M_0. The schematic of the DAC is given in Fig. 9. The duration of the simulation is 3 recovered clock cycles.

DAC (digital-to-analog converter): The DACs directly supply the driving currents to the associative nerves to serve as a stimulus. The amplitude of the current is determined by the MAG field of the incoming packet. The widths of the MOS's controlled by M_i's as well as the associative mirroring currents are binary-weighted. The D bit determines the direction of the overall current which indicates the sign of the stimulus.

III. SIMULATION AND IMPLEMENTATION

The chip is designed by using the TSMC 0.35 μm 2P4M CMOS process. The layout is shown in Fig. 10.

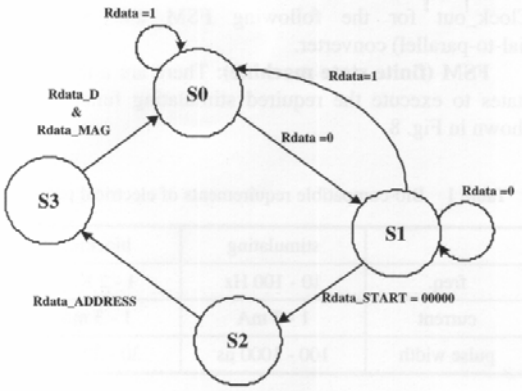

Fig. 8 State transition of the FSM.

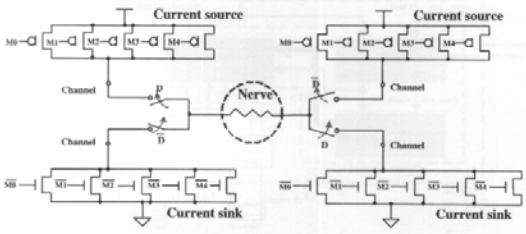

Fig. 9 Interface of DAC and the nerve.

Fig. 11 is the worst-case post-layout simulation given the SS model, at 36°C. Fig. 12 is the post-layout simulation by PowerMill. Channel 2 is selected to generating a 1.38 mA stimulating current lasting for 600 μs given the testing condition of TT model, 25°C, VDD = 3.3 V. Fig. 13 shows a consecutively 2-channel stimulating scenario with negative currents given as the worst testing condition of SS model, 75°C, VDD = 3.0 V. The characteristics of the proposed design is tabulated in Table 2.

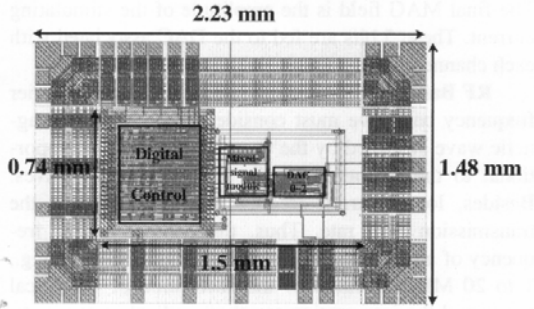

Fig. 10 Layout of the proposed baseband.

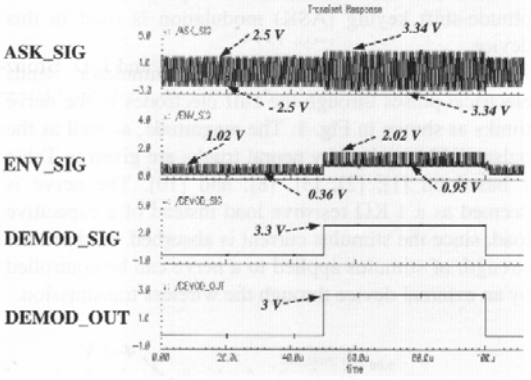

Fig. 11 Post-layout simulation result of ASK demodulator (SS, 36°C).

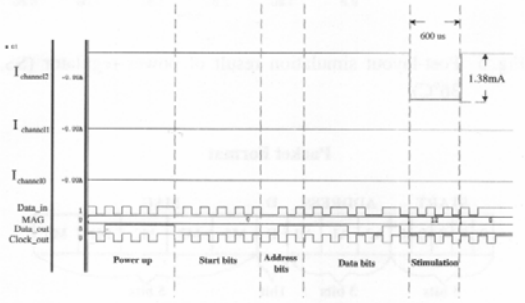

Fig. 12 Post-layout simulation result at a normal condition.

The comparison of the proposed design with several prior works is summarized in Table 3. Our design outperforms in nearly every category. A performance measure is proposed as $E = \frac{I \times t}{size \times power}$ for a microstimulator, which is also given in the last row of Table 3. The proposed design is superior, since [9] is a penetrating device.

IV. CONCLUSION

An SOC-based solution for implantable neural interfacing baseband design is presented. By taking advantage of the advanced processing technologies and the EDA tools, the system-level integration is carried out to explore the feasibility of bio-chip designs. The post-layout simulation results verify the correct functionality as well as the impressive performance.

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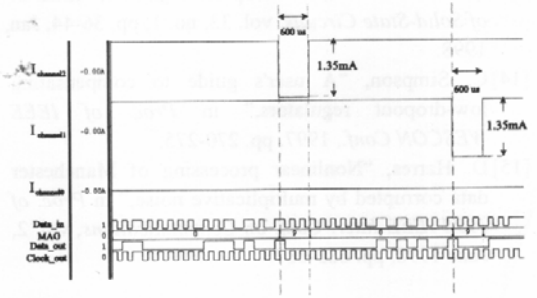

Fig. 13 Post-layout simulation result at the worst condition.

Table 2 Characteristics of the proposed design.

Technology	0.35 μm 2P4M CMOS
Max. bit rate	10 Kbps
Power	5 mW @ 5 MHz
Chip area	2.23 ×1.48 mm^2
Core area	1.50 × 0.74 mm^2
Max. O/P current	1.38 mA
#Channels	3

Table 3 Comparision with prior works.

	[7]	[9]	ours
size (mm^2)	16 × 2	4.4 × 2.5	2.23 × 1.48
output signal (I × t)	30 mA × 514 μs	0.254 mA × 2 ms	1.38 mA × 600 μs
max. power	510 mW	80 μW	5 mW
#Channels	1	2	3
implabtable	Yes	No	Yes
E	0.95	568.18	50.18

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