A 4-kB 500-MHz 4-T CMOS SRAM Using Low-V_{THN} Bitline Drivers and High-V_{THP} Latches

Chua-Chin Wang, *Member, IEEE*, Yih-Long Tseng, Hon-Yuan Leo, and Ron Hu

***Abstract*—The design and physical implementation of a prototypical 500-MHz CMOS 4-T SRAM is presented in this work. The latch of the proposed SRAM cell is realized by a pair of cross coupled high-V_{THP} pMOS transistors, while the bitline drivers are realized by a pair of low-V_{THN} nMOS transistors. The wordline voltage compensation circuit and bitline boosting circuit, then, are neither needed to enhance the data retention of memory cells. Built-in self-refreshing paths make the data retention possible without the appearance of any external refreshing mechanism. The advantages of dual threshold voltage transistors can be used to reduce the access time, and maintain data retention at the same time. Besides, a new design of cascaded noise-immune address transition detector is also included to filter out the unwanted chip select glitches when the SRAM is asynchronously operated.**

***Index Terms*—4-T SRAM, ATD, dual-threshold, SRAM.**

I. Introduction

ALTHOUGH conventional 6-T SRAMs [1] are easily embedded in logic LSIs owing to its compatibility with the CMOS logic process, they are not economical to be included in practical systems due to the large cell area [2]. Takeda *et al.* proposed a smaller 4-T SRAM cell and macro [3]. As pointed by [4], the loadless design of the 4-T SRAMs, [3], [5], requires special process to reduce the threshold voltage of pMOS in order to increase the supply current. Otherwise, the self-refreshing operation is failed due to the leakage current. In short, the wordline-controlled pMOS transistors provide poor driving capability. The design proposed in [4] demands a second power supply voltage, $V_{\mathrm{DD}}+\Delta V$, to precharge the bitline in order to resolve the refreshing of the weak "1" of the storage node. Besides, the access time of the cell in [4] will not as fast as conventional 6-T SRAM cell. A wordline-voltage-level compensation (WLC) is required for data retention. MoSys, Inc., announced an astonishing 1-T SRAM [2] which was claimed to be portable to SOC applications. The 1-T SRAM cell is basically a planar DRAM cell [6] with a special linearization biasing scheme and a sophisticated refreshing controller. Although the area is dramatically reduced, the tradeoff includes multiple voltage sources, alignment precision, and high soft-error rate. On top of these problems, the accessing speed is also slowed down, which is estimated around 300 MHz at 1.8 V and 0.18-μm CMOS process. In this paper, we propose a novel P-latch N-drive 4-T SRAM cell which eliminates the WLC and improves the accessing speed of the SRAM while a built-in self-refreshing path makes the data retention feasible without any externally added refreshing control circuit. Basically, low-V_{th} transistors are used as bit line drivers and high-V_{th} transistors are the data latch components. Not only can the access time be shortened, the data retention is also enhanced. The maximum operation frequency of the SRAM with our proposed design is physically measured to be 500 MHz given the worst-case condition.

TABLE I
THRESHOLD VOLTAGES OF THREE TYPES OF nMOSs/pMOSs, MEDIUM-V_{th} (LOW-V_{th} pMOS IS NOT AVAILABLE IN TSMC 0.18-μm CMOS PROCESS)

	high-V_{th}	medium-V_{th}	low-V_{th}
PMOS	V_{thNoP} = -0.438 V	-0.128 V	V_{thNaP} = N/A
NMOS	V_{thNoN} = 0.445 V	0.269 V	V_{thNaN} = -0.018 V

II. High-Speed 4-T SRAM Design

Although a 4-T SRAM cell was proposed to realize an embedded macro for system-on-a-chip (SOC) applications [3], the intrinsic poor driving capability of wordline-controlled pMOSs deteriorates the access time [7]. Hence, extra sophisticated circuitry is required to neutralize such a problem.

A. Dual-V_{th} Effection of Drain Current

Conventional CMOS processes only provide transistors with single threshold voltage. However, the evolution of CMOS technology makes dual threshold voltage transistor available nowadays. In this paper, dual threshold voltage transistors are utilized in our design using TSMC 0.18-μm CMOS process. In the following text, we will introduce the characteristics of dual threshold transistors. The drain current in the saturation region of a MOSFET transistor is

$$I_D = \frac{k_p}{2}\frac{W_{\mathrm{eff}}}{L_{\mathrm{eff}}}(V_{\mathrm{GS}}-V_{\mathrm{th}})^{\bar{\alpha}} \tag{1}$$

where k_p is a process parameter, and W_{eff} and L_{eff} are effective width and length of the transistor, respectively. In the submicron processes, $\bar{\alpha}$ is about 1.3 to 1.5 [8], [9]. According to (1), a lower threshold voltage can produce a larger drain current.

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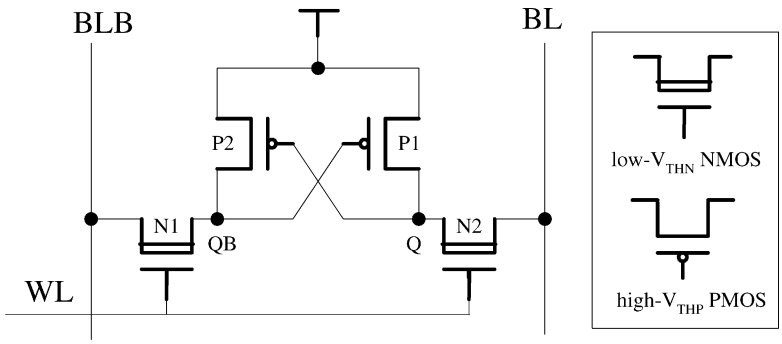

Fig. 1. Proposed 4-T SRAM cell.

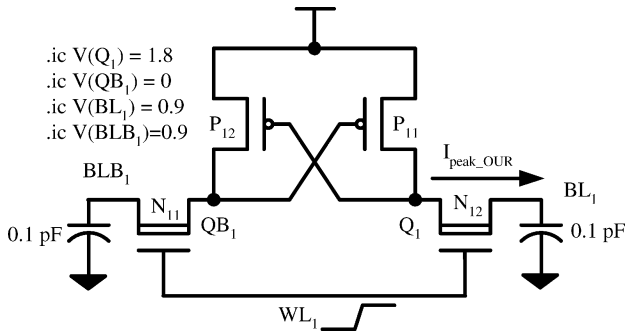

Fig. 2. Peak drive current test schematic of our proposed 4-T SRAM cell.

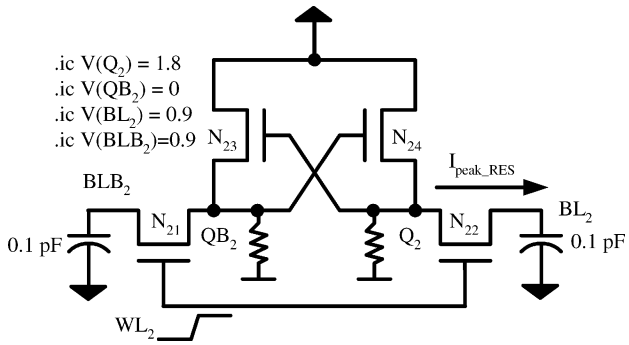

Fig. 3. Peak drive current test schematic of conventional resistance load 4-T SRAM cell [1].

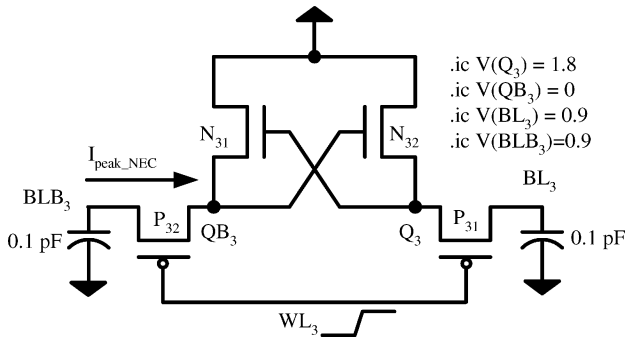

Fig. 4. Peak drive current test schematic of the NEC 4-T SRAM cell [3].

Meanwhile, if we assume $W_{\text{eff}}/L_{\text{eff}}$ as a constant, and choose $\bar{\alpha}$ to be 1.5, then (1) can be simplified as

$$I_D \propto (V_{\text{GS}} - V_{\text{th}})^{1.5}. \tag{2}$$

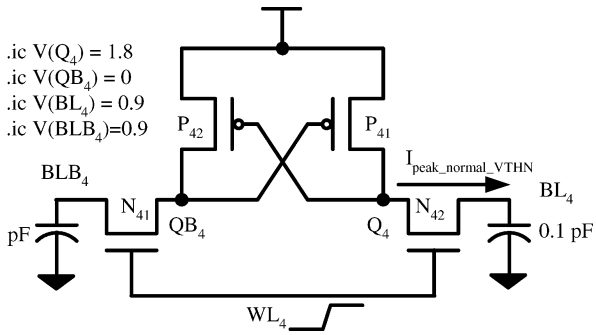

Fig. 5. Peak drive current test schematic of the normal-V_{THN} nMOS-drive pMOS-latch 4-T SRAM cell.

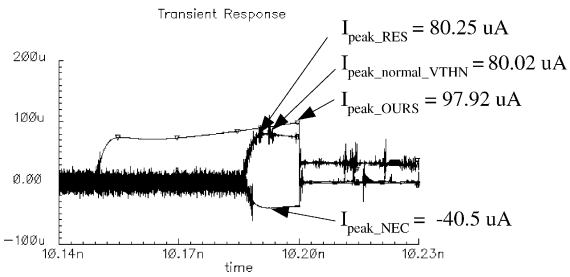

Fig. 6. Waveform of the peak drive currents.

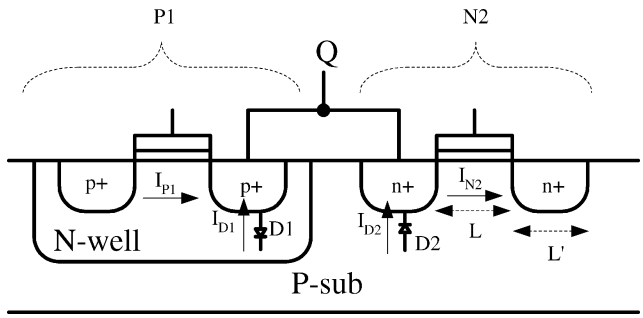

Fig. 7. Sideview of the proposed cell.

In this paper, TSMC 0.18-μm CMOS process is adopted to realize dual threshold voltage transistors. The threshold voltages of high-V_{th} nMOS/pMOS and low-V_{th} nMOS are tabulated in Table I. When $V_{\text{GS}} = V_{\text{DD}} = 1.8$ V, high-threshold voltage of nMOS is $V_{\text{thNoN}} = 0.445$ V, and low-threshold voltage of nMOS is $V_{\text{thNaN}} = -0.018$ V. High-threshold voltage for pMOS is $V_{\text{thNoP}} = -0.438$ V. Thus, let I_{DH} and I_{DL} be the drain currents of the high-threshold voltage transistor

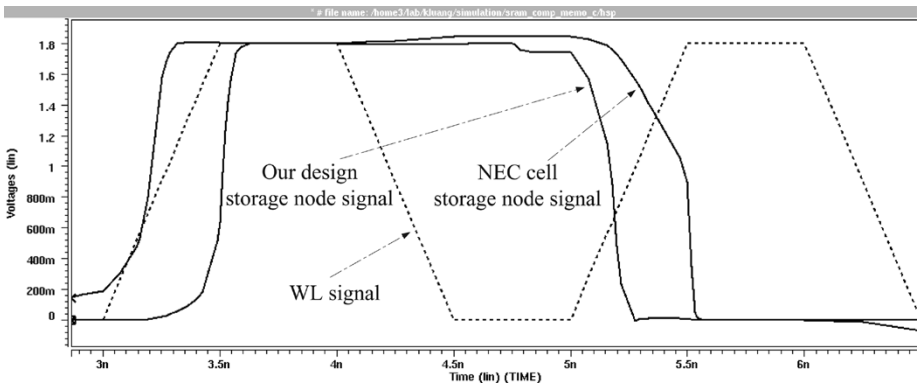

Fig. 8. Waveforms of the proposed cell and the NEC cell.

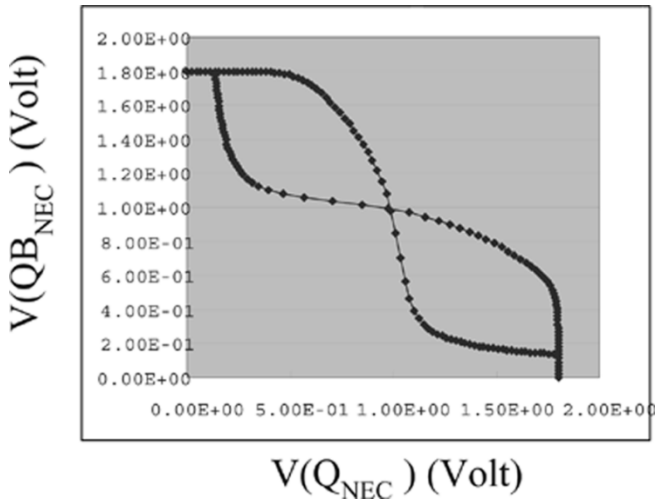

Fig. 9. Static noise margin of NEC cell (1.8 V, 25°C, TT model).

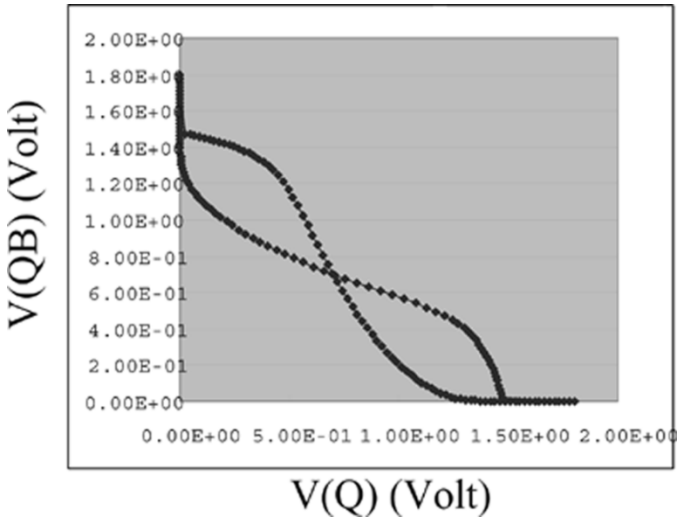

Fig. 10. Static noise margin of the proposed cell (1.8 V, 25°C, TT model).

and low-threshold voltage transistor. We can compute a ratio of $I_{\mathrm{DH}}/I_{\mathrm{DL}}$ as

$$\frac{I_{\mathrm{DH}}}{I_{\mathrm{DL}}} = \frac{\frac{k_p}{2}\frac{W_{\mathrm{eff}}}{L_{\mathrm{eff}}}(V_{\mathrm{GS}} - V_{\mathrm{thNoN}})^{1.5}}{\frac{k_p}{2}\frac{W_{\mathrm{eff}}}{L_{\mathrm{eff}}}(V_{\mathrm{GS}} - V_{\mathrm{thNaN}})^{1.5}} \tag{3}$$

$$= \frac{(V_{\mathrm{GS}} - V_{\mathrm{thNoN}})^{1.5}}{(V_{\mathrm{GS}} - V_{\mathrm{thNaN}})^{1.5}} \tag{4}$$

$$= \frac{(1.8 - 0.445)^{1.5}}{(1.8 - (-0.018))^{1.5}} = \frac{1.577}{2.451} \tag{5}$$

$$\text{Current Increase} = \frac{I_{\mathrm{DL}} - I_{\mathrm{DH}}}{I_{\mathrm{DH}}} \tag{6}$$

$$= \frac{2.451 - 1.577}{1.577} \tag{7}$$

$$\approx 55.42\%. \tag{8}$$

Hence, the theoretical drain current increasing rate of low-V_{th} is about 55.42%.

B. Subthreshold and Leakage Currents of Dual-V_{th} Transistors

With the decreasing of the transistor operating voltage, the threshold voltage is decreasing as well. Hence, the analysis of the subthreshold current is very important. The subthreshold current is given as

$$I_{\mathrm{DSUB}} = \frac{W_{\mathrm{eff}}}{W_o} \cdot I_o \cdot 10^{(V_{\mathrm{GS}} - V_{\mathrm{th}})/S} \tag{9}$$

where W_o and I_o are reference channel width and current level to determine the threshold voltage of an MOS transistor [10]. S is the subthreshold swing parameter which can be calculated as

$$S \approx 2.3 V_{\mathrm{T}} \left[1 + \frac{C_d}{C_{\mathrm{ox}}}\right] \tag{10}$$

TABLE II
PERFORMANCE COMPARISON OF SRAM CELLS (Load = 0.8 pF, Temp = 25°C)

delays	NEC SRAM cell [3]	ours
rise propagation delay	270 ps	-56 ps
fall propagation delay	269 ps	-77 ps
rise delay	131 ps	215 ps
fall delay	289 ps	146 ps

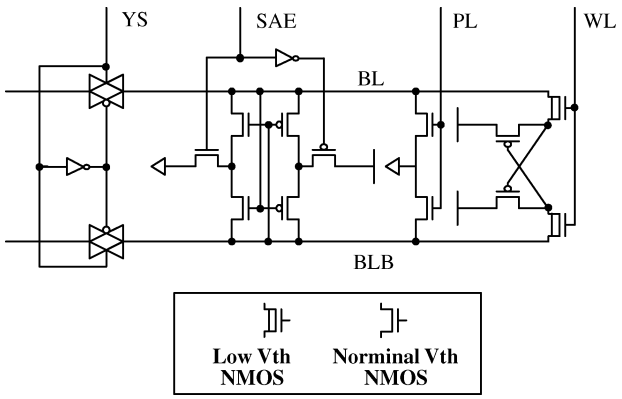

Fig. 11. Predischarging circuitry, SA, and the cell.

TABLE III
COMPARISON OF PRECHARGING TIME AND PREDISCHARGING TIME
(Load = 0.8 pF, Temp = 25°C)

delays	NEC SRAM cell [3]	ours
propagation delay	106.9 ps	51.61 ps
fall/rise delay	198.0 ps	86.65 ps

where $V_{\rm T}$ is thermal voltage, and C_d is the junction capacitance between source and drain. The leakage current can be obtained by replacing $V_{\rm GS}$ with 0, which is

$$I_{\rm leak} = \frac{W_{\rm eff}}{W_o} I_o 10^{-V_{\rm th}/S}. \tag{11}$$

If W_o remains unchanged, $I_{\rm DSUB}$ as well as $I_{\rm leak}$ will be increased when I_o increases. Thus, the subthreshold current becomes a positive factor of driving wires. In short, a transistor with low $V_{\rm th}$ is more appropriate to drive wire rather than to store data.

According to the discussion in the above, we conclude the following.

- High-$V_{\rm th}$ transistors possess the advantage of low leakage current. Hence, they are appropriate to **store data** in memory designs.
- Low-$V_{\rm th}$ transistors possess a larger drain current. Therefore, it is more suitable to **drive** the bit lines.

By taking advantages of these two kinds of transistors, a refined design of SRAM memory cell is proposed.

C. Proposed SRAM Cell

Referring to Fig. 1, a P-latch N-drive 4-T SRAM cell is proposed to resolve all of the difficulties mentioned in the prior works. The data are kept in the back-to-back pMOS pair. N1 and N2 are, respectively, the bitlines (BL, BLB) drivers which are controlled by the word line (WL). If the threshold voltage of N1 and N2 is low, the switching time of N1 and N2 will be reduced which will in turn shorten the access time of the SRAM cell. Hence, we use low-$V_{\rm th}$ nMOS provided by TSMC 0.18-μm 1P6M process to implement the driving transistors. It will produce more driving current than medium-$V_{\rm th}$ or high-$V_{\rm th}$ transistors.

Figs. 2–5, respectively, show the schematics of four different 4-T SRAM cell designs (our proposed SRAM cell, resistance load 4-T SRAM cell [1], nMOS-latch pMOS-drive NEC 4-T SRAM cell [3], and normal-$V_{\rm THN}$-nMOS-drive pMOS-latch 4-T SRAM cell) to derive their drive peak current. Fig. 6 shows the overall comparison of the drive peak currents of the SRAM cells in a read operation. The peak current of our proposed SRAM cell is 97.92 μA, which is at least 25% better than all of that of the other 4-T SRAM cells.

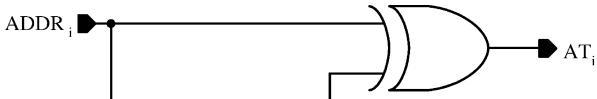

Fig. 12. Stage 1 (the usual ATD design).

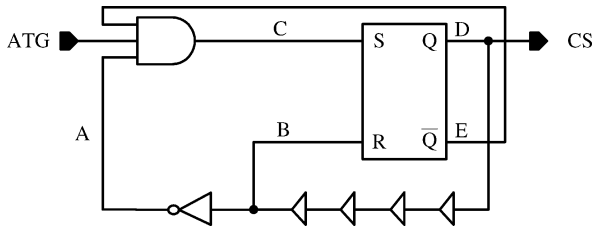

Fig. 13. Stage 2 of the proposed ATD.

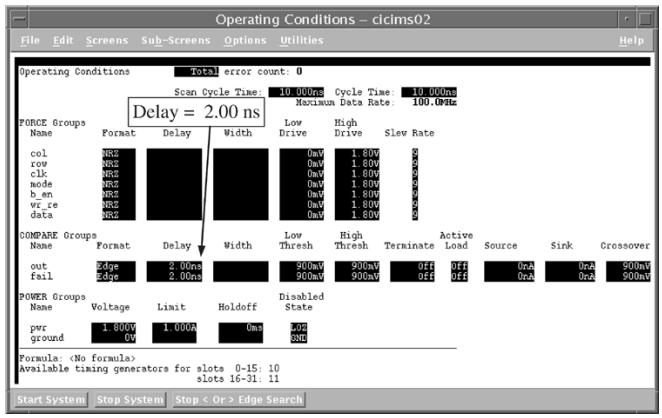

Fig. 14. Ideal ATD wavefoms for asynchronous operations.

By contrast, transistors with high $V_{\rm th}$ process low leakage current and subthreshold current. Thus, they are very good to be cross coupled as a data latch as shown in Fig. 1. We then use high-$V_{\rm th}$ transistors, i.e., P1 and P2, to keep valid data. It is also well known that such a pseudolatch still possesses the leakage problem which leads to the loss of the stored data. The leakage can be neutralized by "hidden self-recharging path," predischarged to VSS referring to Fig. 7, assume that N1, N2 are off given that $\rm WL = 0$. There are four currents affecting the voltage level of node Q when the data node Q is floating

$$\text{subthreshold current} : I_{P1} \text{ and } I_{N2}$$
$$\text{reverse bias current} : I_{D1} \text{ and } I_{D2}.$$

The requirement of the data retention for the possible weak "0" at node Q is $(I_{P1} + I_{D1}) < (I_{N2} + I_{D2})$. Notably, the

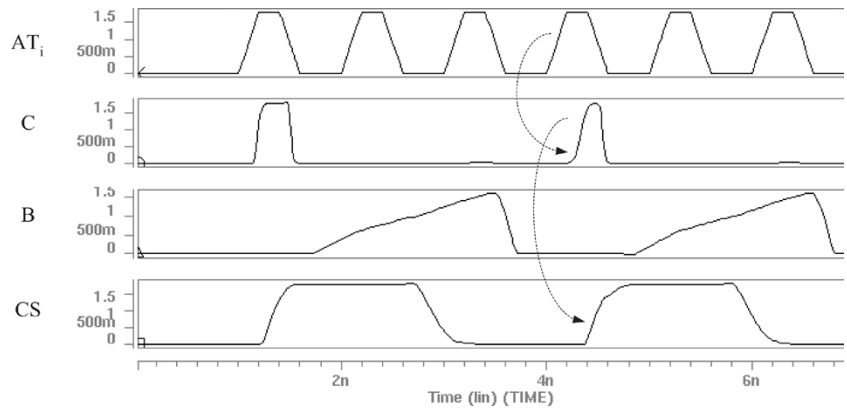

Fig. 15. Simulation results of the proposed ATD.

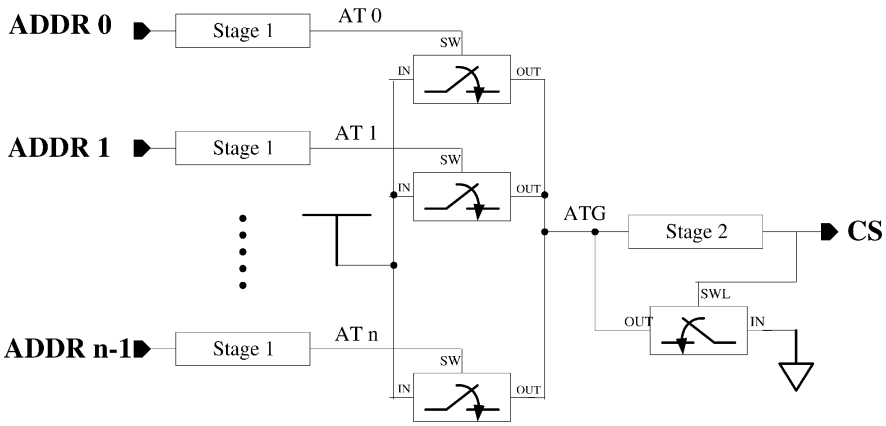

Fig. 16. Overall cascaded ATD design.

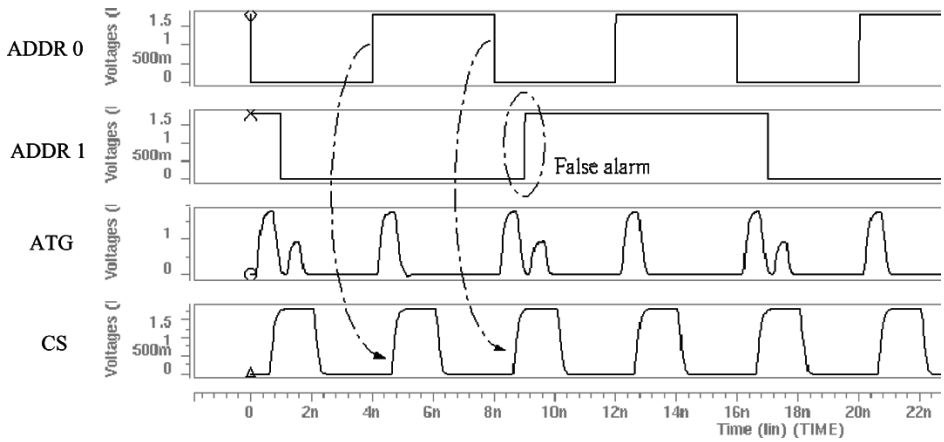

Fig. 17. ATD response at the presence of an false-alarm signal.

magnitude of the subthreshold currents are adjustable according to the following:

$$I_{\mathrm{sub}} = \frac{W}{L} e^{(V_{gs}-V_t)/nV_{\mathrm{T}}}(1 - e^{-V_{ds}/V_{\mathrm{T}}}) \tag{12}$$

$$I_D = WL' \cdot I_S(e^{V/V_{\mathrm{T}}} - 1) = I_{\mathrm{leakage}} \tag{13}$$

where L and L' denote the widthes of the gate and the parasitic diode, respectively. Thus, the data retention problem can be resolved by solving the W/L ratios to meet the requirement of $(I_{P1} + I_{D1}) < (I_{N2} + I_{D2})$. Fig. 8 reveals the comparison of the NEC SRAM cell and ours. Table II tabulated different delay figures of the NEC SRAM cell and ours. Notably, the transition time of $(1/2)V_{\mathrm{DD}}$ of our design storage node signal is leading the word line signal. Hence, the rise propagation delay of ours is denoted with "-" signal. NEC SRAM cell has better performance of static noise margin as shown in Fig. 9. The proposed SRAM cell has acceptable static noise margin as shown in Fig. 10.

The latch MOSs of the proposed SRAM cell are pMOSs. Hence, BL and BLB must be predischarged to VSS at the standby operation as a pull-down path for the proposed SRAM

TABLE IV
ENERGY-DELAY COMPARISON OF SRAM CELLS

	delay (input 10% to output 50%)	power consumption	energy-delay product
NEC SRAM cell [3]	0.47 ns	9.8 μW	4.606 μW-ns
ours	0.12 ns	15.3 μW	1.836 μW-ns

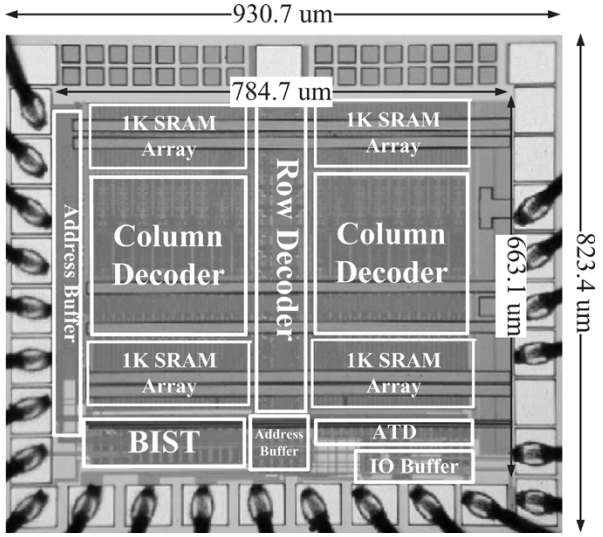

Fig. 18. Die photo of the proposed SRAM.

cell. As shown in Fig. 11, PL is the discharging signal to ground BL and BLB in nonaccessing durations.

The mobility of nMOS is about twice than that of pMOS given the same length and width. Hence, the predischarging time is roughly half of the precharging time. The SRAM access time is, thus, reduced by the predischarging scheme. Table III shows that the speed-up ratio of the predischarging scheme is twice as fast as the NEC SRAM cells. Becides operation speed, power is also an important concern. In order to compare on the fair basis, the comparison of power, delay, and energy-delay product between the proposed SRAM cell and the NEC SRAM cell is summarized in Table IV. The proposed design has a better performance with regard to both delay and energy-delay product.

D. Cascaded Noise-Resistant ATD

An address transition detector (ATD) is required to initiate a memory read/write operation asynchronously. As soon as the address lines on the bus are detected to reveal a significant variation, a chip select (CS) signal is asserted to enable the memory. The advantages of such a method are obvious, i.e., power-saving, pin-saving, and high-speed. Drawbacks of prior ATD designs were addressed in [11]. By contrast, the ATD in [11] has its own problem which is the large area due to the delay elements. We, thus, propose a cascaded ATD which is composed of Stage 1 and Stage 2 described in the following text to overcome all of the mentioned problems.

- Stage 1: As shown in Fig. 12, a typical address transition detector for each address line is used. The AT_i signal (address transition), where $i \epsilon 0, \ldots, n-1$, will be very vulnerable to glitches and noises at the address line since the XOR gate is transparent.
- Stage 2: Fig. 13 shows the ATD to filter any unwanted glitches or noises coupled in the ATG which is the granted AT_i signal. The design comprises a SRFF and a delay buffer, BUFF2. The feedback loop stabilizes the meaningful CS signal. BUFF2 is used to predetermine the width of the CS strobe such that any perturbation occurring in the duration of the strobe is ignored. The operation is summarized as follows.

1) After initialization, A and E are set to high, C, CS, and B are low.
2) As soon as one ADDR_i is switched, AT_i will be high. If anyone of the AT_i's is high, the ATG will be high, and the C will be turned high. $\mathrm{C} = 1$ sets Q of the SRFF, i.e., CS and D. Meanwhile, E is low which then turns C low through the feedback loop.
3) The W/L of the inverters in BUFF2 is adjustable which determines the transient voltage at B. The rise time at B is the duration that CS remains high, while the fall time at B equals to the time that the CS can be turned high again after it is switched low. An ideal operation waveform is given in Fig. 14. Comparing to the ATD of [11], Stage 2 of [11] needs two delay chains, two 2-input-NORs, two inverters, and an nMOS. By contrast, Stage 2 of the proposed design only needs one delay chain, one 3-input-NAND, one inverter, and a SRFF (six transistors). The major improvement of the proposed ATD is saving a delay chain.

Fig. 15 is the simulation waveform of Stage 2 when AT_i is coupled with unwanted glitches. These glitches or false-alarm pulses are all rejected. The entire ATD is shown in Fig. 16. Since all of the address lines will not be switched simultaneously, Stage 2 is required to keep the SRAM operating correctly in the asynchronous mode. Fig. 17 is the simulation waveforms given a false-alarm address transition.

III. PROPOSED SRAM CELL SIMULATION AND PHYSICAL TESTING

The proposed design is implemented by TSMC 0.18 μm 1P6M CMOS technology which is a digital logic process. Besides the usual synchronous mode and asynchronous mode, which the ATD is enabled, the proposed memory also comprises a BIST mode. Fig. 18 is the die photo of the proposed SRAM. The chip area is 930×823 $\mu\mathrm{m}^2$.

A. Proposed SRAM Cell and Noise Analysis

The specifications of the proposed 4 kB SRAM is summarized in Table V. Fig. 19 shows the post-layout simulation results of the proposed 4-T SRAM. They are generated by the TimeMill and CADENCE tools. The SRAM cells may have function errors due to process variations, MOS size mismatches, temperature variations, pulse noise, or V_{DD}/GND noise. It is a must to

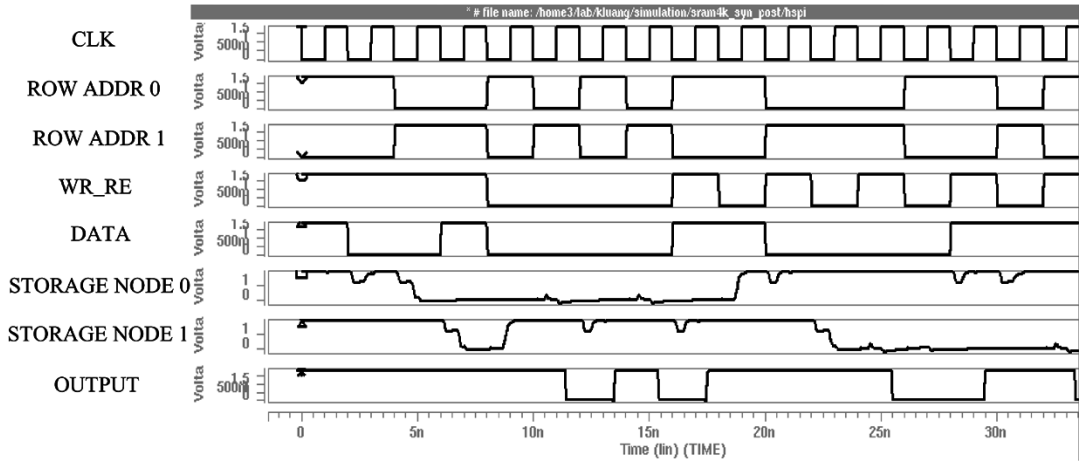

Fig. 19. Post-layout simulation results.

TABLE V
4-kB 4-T SRAM SPEC IN DIFFERENT MODES

	Synch.	Asynch.	BIST
clock	500 MHz	250 MHz	100 MHz
access delay	2.49 ns	4.1 ns	10.0 ns
avg. power	152 mW	71.1 mW	15.8 mW
max. power	818 mW	825 mW	346 mW
VDD	1.8±0.2V	1.8±0.2V	1.8±0.2V

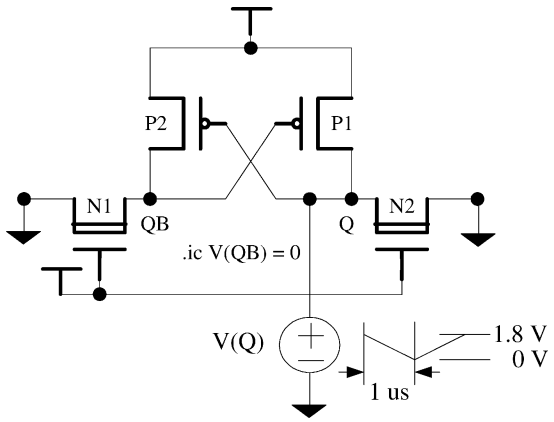

Fig. 20. Test circuit for static noise margin.

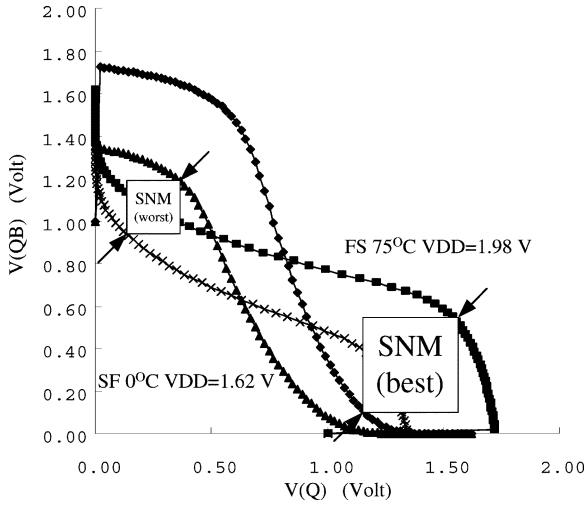

Fig. 21. Static noise margin.

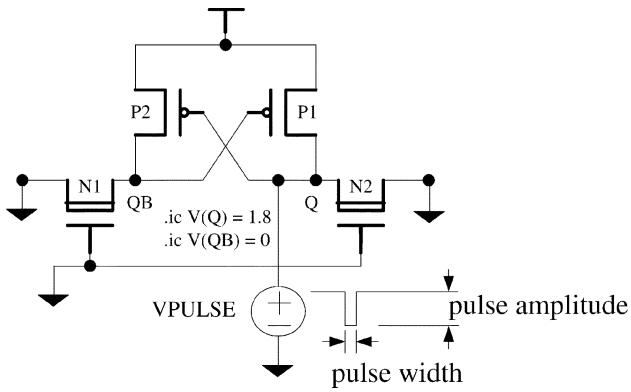

Fig. 22. Test circuit for dynamic noise margin.

analyze the noise effect and SRAM cell stability. In general, we can summarize the dc noise effect by static noise margin (SNM) analysis, and summrize the pulse noise effect by dynamic noise margin (DNM) analysis. When analysing the static noise margin of the proposed SRAM cell, we use the test circuit shown in Fig. 20 to simulate the 16 corners (SS, SF, FS, FF) $\times$ (0°C, 75°C) $\times$ ($V_{\mathrm{DD}} + 10\%$, $V_{\mathrm{DD}} - 10\%$). As shown in Fig. 21, the best static noise margin (SF, 75°C, $V_{\mathrm{DD}} + 10\%$) is 566 mV. The worst case (FS, 0°C, $V_{\mathrm{DD}} - 10\%$) is 212 mV. The worst case of the statice noise margin still meets the 200 mV requirement of 0.18-μm process [8], [12]. When analysing the dynamic noise margin of our proposed SRAM cell, we use the test circuit shown in Fig. 22. The shmoo plot of the dynamic noise margin is shown in Fig. 23.

TABLE VI
SIMULATION OF THE OPERATION CLOCK RATE AND POWER CONSUMPTION

Operation Mode	Max clock rate	Average Power
Synchronous mode	500 MHz	152 mW (500 MHz)
Asynchronous mode	250 MHz	71.1 mW (250 MHz)
BIST mode	100 MHz	15.8 mW (100 MHz)

TABLE VII
PHYSICAL TESTING OF THE OPERATION CLOCK RATE, POWER CONSUMPTION, AND ESTIMATED POWER CONSUMPTION

Operation Mode	Max clock rate	Average Power	estimated Power
Synchronous mode	500 MHz	44.2 mW (100 MHz)	221 (44.2×5) mW (500 MHz)
Asynchronous mode	333 MHz	39.5 mW (100 MHz)	98.8 (39.5×2.5) mW (100 MHz)
BIST mode	100 MHz	20 mW (100 MHz)	20 mW (100 MHz)

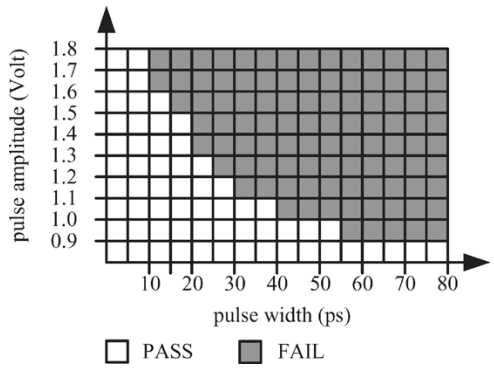

Fig. 23. Shmoo plot for the dynamic noise margin.

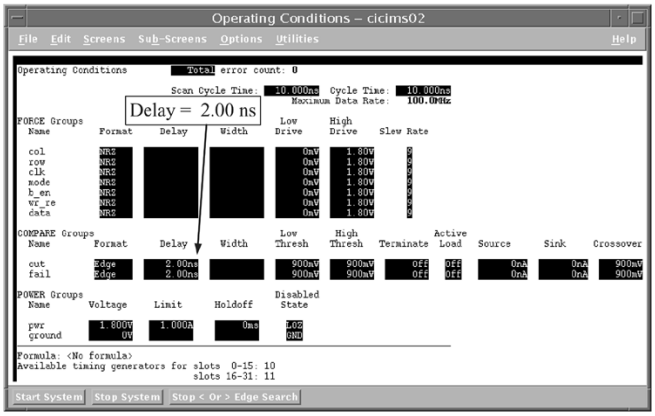

Fig. 24. Synchronous mode operation and the signal-fetch conditions.

B. Physical Testing Results

The proposed design is tested and verified by the IMS200 tester. The functions of the synchronous mode, asynchronous mode and BIST mode has been proved by the testing of continuous read/write of row/column address. Fig. 24 shows the signal-fetch conditions of the synchronous mode, and Fig. 25 is the signal-fetch conditions of the asynchronous operation. Notably, Fig. 24 shows the output data fetch delay is 2 ns, which inidicates the highest operation speed of the proposed design is 500 MHz.

C. Summarization of Simulation and Testing Results

Tables VI and VII summarize the simulation and physical testing results of the maximum clock rate and the average power in synchronous mode, asynchronous mode, and BIST mode. Owing to the linear proportionality between the operation frequency and the power consumption, we can estimate the power consumption at 500 MHz by five times of the power consmption at 100 MHz, which is given in Table VII.

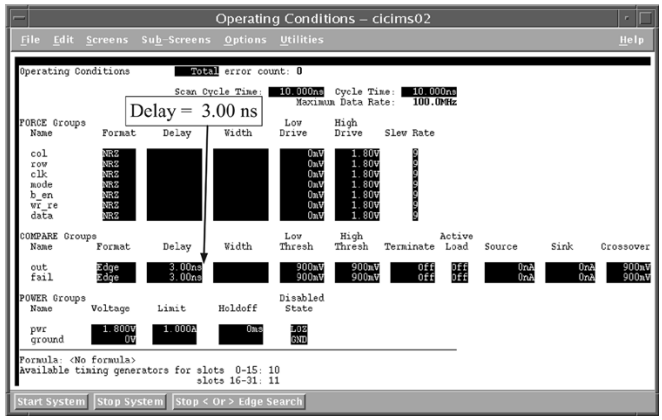

Fig. 25. Asynchronous mode operation and the signal-fetch condition.

IV. CONCLUSION

We have proposed a novel P-latch N-drive 4-T SRAM design by using the dual threshold voltage transistors for high-speed memory designs. The high-V_{th} transistors are used to construct data storage latches, and the low-V_{th} transistors are used to improve driving capability and speed. The proposed design can be fully implemented by a digital CMOS process. Meanwhile, a two-stage ATD design is included to carry out the asynchronous access operation such that the power consumption is reduced.

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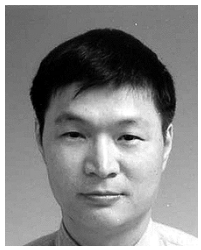

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