# A LOW-COST PLASMA DISPLAY PANEL DATA DISPATCHER FOR IMAGE ENHANCEMENT

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## ABSTRACT

*Plasma Display Panel (PDP) is one of the best solutions for TVsets, but its retail price remains higher than that of CRTs. This paper proposes a low-cost PDP Data dispatcher which focuses on converting the image signal inputs into the PDP display format and reducing the numbers of components and the cost.*

## 1 INTRODUCTION

The Plasma Display Panel (PDP) is a promising selection in the future of the display market. It has advantages including thin, wide view angle, and no distortion from magnetic fields. A critical factor for PDP suppliers to be successful is to reduce the overall production cost. Lower price attracts entertainment and business applications, e.g., TV sets. Many efforts have been applied to improve the Plasma Display driving methods [1], [2], phosphor [16], cross sectional structure of the panel [15], picture quality [3], [6], [8], [10], [11], [12], [13] and the driver ICs [7]. There are only a few people paying attention to the Plasma Display Panel Data dispatcher [4], [5], which is one of the most important parts in the PDP set (Figure 1). The PDP Data dispatcher is used to convert image data into a PDP driving format. The driving format of PDP shown in Figure 2 is the "Address Display Separate" (ADS) method, which is composed of Erase period, Address period and Sustain period [8]. The PDP displays 8-bit gray scale, based on the ADS method (also called binary-coded light-emission-period [8]). One TV frame consists of 8 sub-fields and each sub-field represents a portion of brightness. In general, the dispatcher consumes 10% of the PDP prime cost. Most of the PDP manufactures design this dispatcher using 4 or 5 advanced and large FPGAs as shown in Figure 3. In this paper, we propose a low-cost PDP Data dispatcher with an image enhancement method. The proposed architecture can also be integrated as an SOC chip for PDPs in the future to reduce the overall cost.

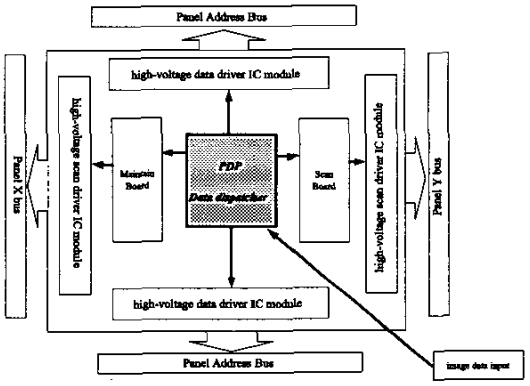


Figure 1: The entire Plasma Display Panel System

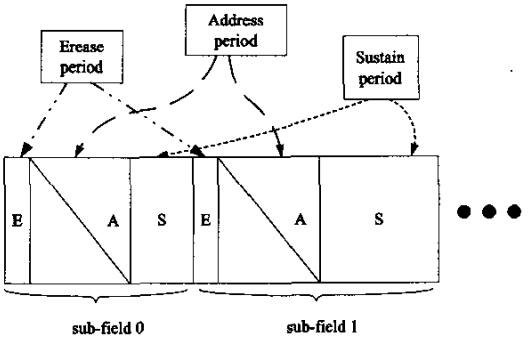


Figure 2: Address Display Separate method

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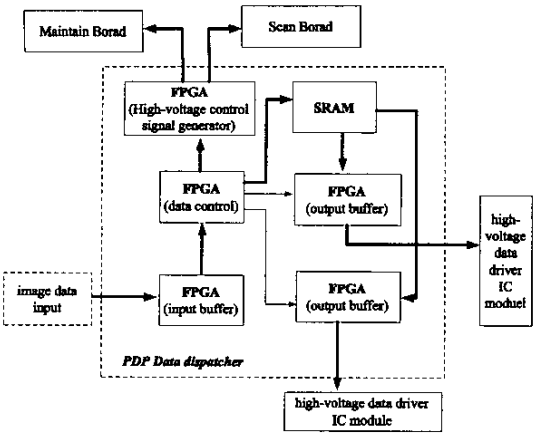


Figure 3: The conventional Plasma Display Panel Data dispatcher

## 2 PLASMA DISPLAY PANEL DATA DISPATCHER

Most of PDP Data dispatchers use large input buffers to convert image signals into the format reqired by high-voltage data driver IC (HVDIC). Meanwhile, these data are stored in the SDRAM modules. The data in SDRAMs are rearranged by output buffers for the display at last. In other words, too many registers are used in data transformation among the input signals, the input buffers, the SDRAMs, and the output buffers. We propose a novel design to reduce these I/O buffers, by using SRAMs instead of SDRAMs to achieve the same converting functions while alleviating the so-called "dynamic false contours" problem. This method can reduce 80% of input buffer registers and 50% of output buffer registers. It also can shorten the data processing time by appropriate data arrangement. The PDP Data dispatcher consists of an Average Picture Level (APL) module, an 8-to-10 subfield translator, a control module, an output buffer module, SRAM modules, and a High-voltage control signal generator. Figure 4 shown the entire proposed PDP dispatcher architecture.

### 2.1 Input data format

The input data is following the VESA Monitor Timings Standard, which contains vertical synchronize (V-sync), horizontal synchronize (Hsync), CLKin, Data Enable (DE), and 8 bits for R, G, and B.

### 2.2 Average Picture Level (APL) module

The Average Picture Level(APL) module determines the brightness of the image. It will reduce the afterimage and image sticking effects, and also can increase phosphor's lifetime if the brightness is larger than a pre-determined threshold. Every unit of the input image data are composed of R, G, and B has 8-bit width. The strength of R, G, and B (8 bits, $0 \sim 255$) is divided into 32 levels. We tend adopt a min-max method to determine the average brightness of the current image instead of using any physical mathematical operations. The strength of R. G and B is divided into 32 levels. For instance, level 0 denotes $0 \sim 7$, level 1 denotes $8 \sim 15$, $\cdots$ and so on. 32 counters are used to record and accumulate how many units possessing the same level of brightness for each R, G, B, as shown in Figure 5. After one frame is fully read and processed, the counters keeping the maximum number will be dumped to the final comparator which in turn selects the minimum of the maximum outputs of R, G, and B. The advantage of such a min-max method is to avoid any multiplication or division operations. In short, the APL output is the minimum among R, G, and B maximums. The output is sent to the "High-voltage control signal generator" module. The High-voltage control signal generator module chooses the additional or reducible sustain pulse from the table in the ROM of Figure 4 basing on the APL output value. Figure 5 is the entire APL architecture.

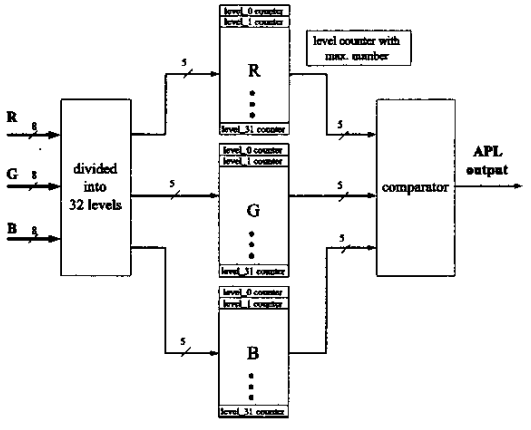


Figure 5: The Average Picture Level module

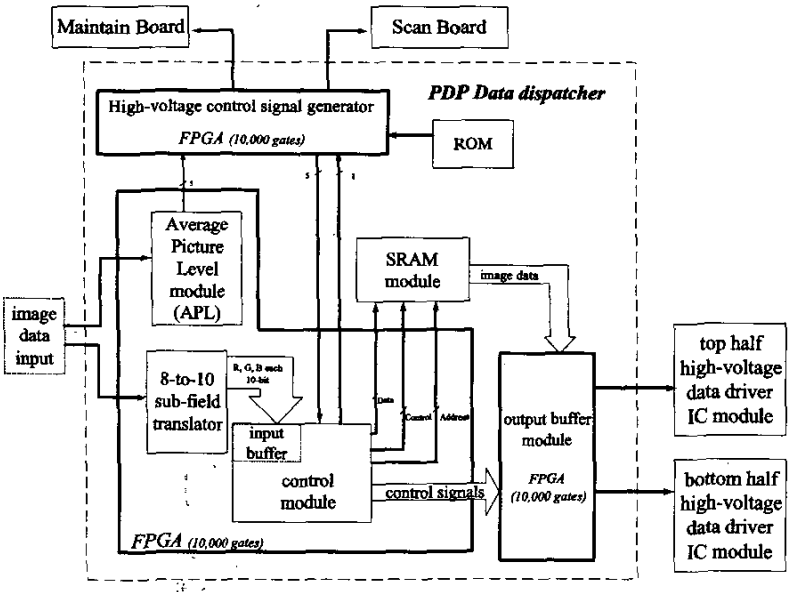


Figure 4: The proposed PDP Data dispatcher

### 2.3 8-to-10 sub-field translator

Most of companies use ADS method to drive the Plasma Display Panel after the method had been publicized in 1990 [17]. Since the ADS method can save numbers of high-voltage driver ICs than non-ADS [9]. Nevertheless, "Address Display Separate" caused a serious image defect named "dynamic false contours" [8], [13]. We reduce the dynamic false contours by increasing and redefining the number of sub-fields from 8 to 10 in the sub-field translator of our design, [14], as shown in Figure 6. Figure 7 and 8 are simulations of retinal reaction to moving pixels. The result of the comparisons between 10 and 8 sub-fields is tabulates on Table 1.

| | 8-bit [8] | 10-bit |
|---|---|---|
| Max. difference on moving pixels from gray level 127 to 128 | 128 | 64 |
| Max. difference on moving pixels from gray level 128 to 127 | 128 | 64 |

Table 1: The difference between 10 and 8 sub-fields on retinal reaction of moving pixels

### 2.4 Control module

We convert the input image data by using the input buffers solely to fit the input format of high-voltage data driver ICs (HVDIC). These converted data are

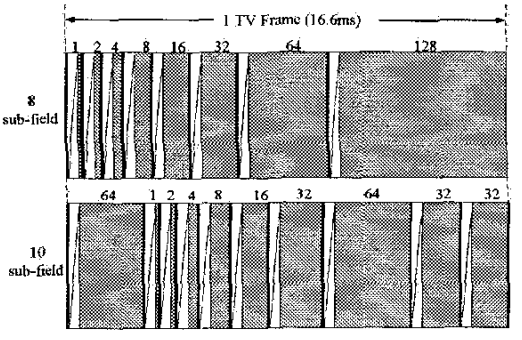


Figure 6: The 8 and 10 sub-field timing diagram

stored in the SRAM module. It required one FPGA to carry out the input buffer in prior works. By contrast, we only utilize a few registers by employing a novel data arrangement method SRAM module which will be described later. The control module is in charge of the timing control of the SRAM module and output buffers, and commanding the High-voltage control signal generator.

### 2.5 SRAM module

One TV frame data will be as large as 12 Mb. In order to display such a huge amount of data in a short period of time ($\leq$ 16.6 ms), the high-voltage data driver IC module is divided into 2 parts, which are respec-

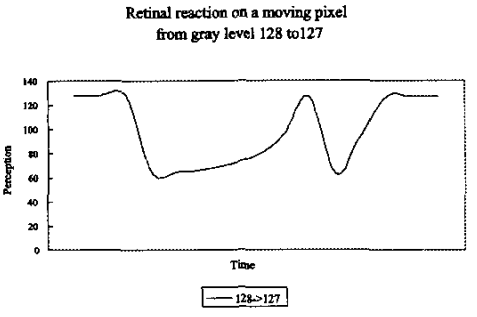


Figure 7: The retinal reaction, moving pixel gray level from 128 to 127

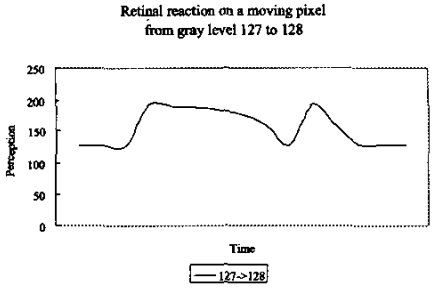


Figure 8: The retinal reaction, moving pixel gray level from 127 to 128

tively in charge of the display operation of the top half and bottom half of the panel. The entire architecture of this PDP Data dispatcher is based on the width of SRAM module. The width of SRAM module is decided by the formula,

$$W = I \cdot D \tag{1}$$

$W$ is each line width of SRAM module. $I$ is the high-voltage data driver IC inputs, and the $D$ is a factor of the number of shift clocks in high-voltage data driver IC. If the width of SRAM module does not fit this formula, the output buffer can not output the received data from the ROM and directly feed the data to high-voltage data driver IC module. We need to re-arrange the data following the correct format of high-voltage data driver IC module. Besides, it also needs to take the required bandwidth of output buffer into consideration. We arrange the data by using 3(high-voltage data driver IC inputs)*8 (a factor of 32)=24 bits as the stored data width. Hence, the output buffer only needs to collect the data. In our design, the data format of the high-voltage data driver IC module interlaces outputs between 2 sections in continuous 64 clocks. For example, the odd-numbered CLKs feed sub-field pixel (R, G, B, 3 bits) 1, 2, 3 $\cdots$ to 32 (in Figure 9), and even-numbered CLKs feed sub-field pixel 33, 34, 35 $\cdots$ to 64 (in Figure 10).

### 2.6 Output buffer

This module stores the data which will be output to high-voltage data driver IC, and send the image data and control signals to high-voltage data driver IC when receiving the address scan fetch signal for the High-voltage control signal generator. The depth of each output buffer register block is the same as the width of SRAM module. Our panel is using dual-scan method to reduce the address period time. Hence, the output buffer module is divided into 4 buffer blocks, where 2 buffer blocks are for top half panel and the other two blocks for bottom half panel. Two buffer blocks alternatively latch and output data. Figure 9 shows the data arrangement in the SRAM module, the required data flow of the HVDIC, and the data arrangement in the output buffer in odd-numbered CLKs to the HVDIC module. Figure 10 shows the data arrangement of output buffer in the even-numbered CLKs to the HVDIC module. Figure 11 shows the data arrangement in the output buffers which does not match the data format of the HVDIC, where the selection of $W$ of the SRAM module does not meet Equ. (1).

### 2.7 High-voltage control signal generator

This module converts driving voltage waveforms into the high-voltage switching components (in the Maintain board and the Scan board as shown in Figure 4) control signal, and then feeds these signals to the Maintain board and the Scan board. Another feature of this module is to accept the APL value and select corresponding sustain pulse value in the ROM.

## 3 COMPARISON

The proposed Plasma Display Panel Data dispatcher consists of 3 10K (10,000 gates)FPGAs. The prior work [4] used 4 10K and 1 20K (20,000 gates) FPGAs. In addition, [4] spent a total of 962.2 $\mu$s. On the other hand, besides the initialization to fill the

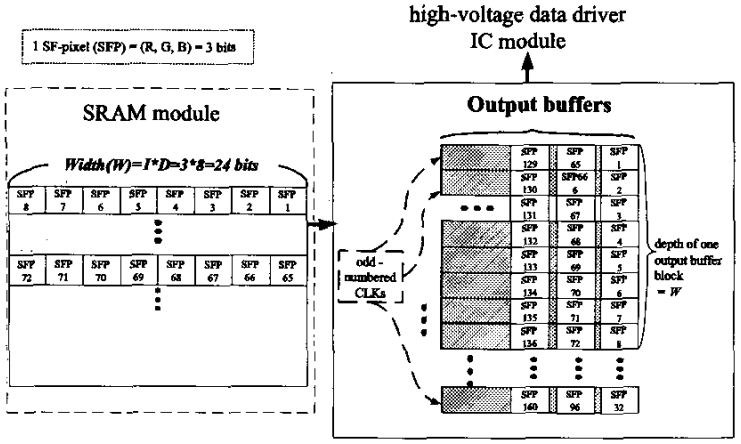


Figure 9: The data arrangement in SRAM module and output buffer in odd-numbered CLKs

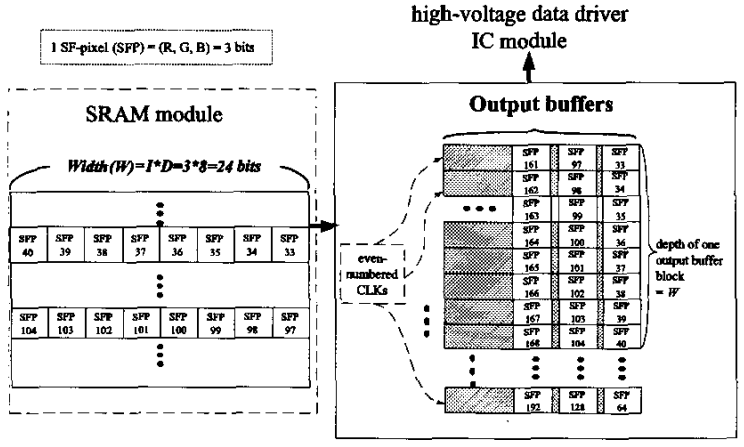


Figure 10: The data arrangement in output buffer in even-numbered CLKs

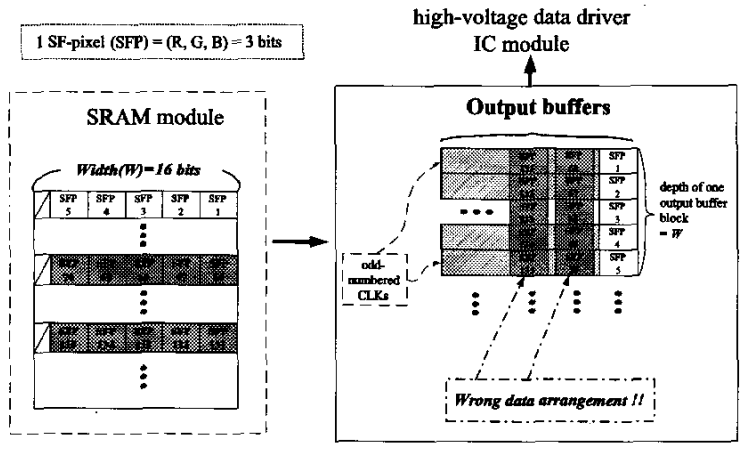


Figure 11: The wrong width selection of the SRAM module

output buffer, our design operates pipelinedly which can continuously send the pixel data to the HVDIC module. Hence, the data processing time is shorten to 350 ns (initialization) + (25 ns*(64+2)*300) = 495.35 $\mu$s. Table 2 tabulates all of the comparisons.

| | prior work [4] | our |
|---|---|---|
| FPGA Count | 5 | 3 |
| logic gates | 600,000 | 300,000 |
| overall memory module | SDRAM (96 Mb) | SRAM (48 Mb) |
| input buffer reg. | 4098 | 480 |
| output buffer reg. | 5120 | 1344 |
| PDP addressing time | 962.2 $\mu$s | 495.35 $\mu$s |

Table 2: The hardware cost analysis

## 4 CONCLUSION

The 42-inch 600*800 pixels PDP displays an improved image shown in Figure 12. Our design reduces 20% of the cost and 50% of the address period time, which in turn increases the sustain period for brightness control. It also reduces the dynamic false contours by increasing the number of sub-field and rearranged the sub-field permutation method.

Figure 12: Improved image on PDP

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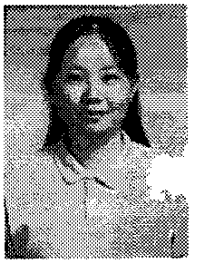
**Biography**

Chua-Chin Wang was born in Taiwan in 1962. He received the B.S. degree in electrical engineering from National Taiwan University in 1984, and the M. S. and Ph. D. degree in electrical engineering from State University of New York in Stony Brook in 1988 and 1992, respectively. He is currently a Professor in the Department of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan. His recent research interests include low power and high speed logic circuit design, VLSI design, neural networks, and interfacing I/O circuits.



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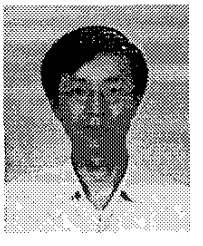

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