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A Practical Load-optimized VCO Design for Low-jitter 5V 500 MHz Digital Phase-locked Loop*

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In high-speed digital systems and high-resolution display devices, the jitter effect of phase-locked loops (PLL) limits the system performance. Power supply noise coupling is one of the major causes of PLL jitter problems, especially with mixed-signal systems. The paper presents a targeted 5.0 V 500 MHz PLL which is implemented by a 0.6 um 1P3M digital CMOS technology. The features of the proposed design include a load-optimized 3-stage VCO, a frequency limiter RC circuit, and a ratioed VCO controlling current mirror. The jitter, thus, is reduced to 72.693 ps at 600 MHz at the presence of supply noise, while the sensitivity is limited to 286.6 ps/V. This high-noise immunity design allows that the PLL can be integrated with digital circuits.

Keywords: Phase-locked loop; VCO; Low-jitter; 1P3M CMOS technology; Load-optimized; VLSI

1. INTRODUCTION

PLLs are often used in the I/O interfaces of digital ICs in order to hide clock distribution delays and improve the overall system timing [5] or high frequency clock generators [2, 3, 7]. However, the noisy environment in which the ICs operate might introduce unwanted jitter from the expected timing at the output of the PLL. With a demand on high frequency and high speed PLLs, the design of low jitter PLLs thus become very challenging. Though many PLL designs have been proposed [1, 4, 6, 7], several design factors have long been ignored. First, the lock time of the PLL should be as short as possible. Second, the lowest output frequency might not necessarily be zero. Third, the size ratio of the conventional ring oscillator type VCO (voltage controlled oscillator) should be tuned and might be the same at every stage of inverters. In this work, we present a PLL design including a load-optimized 3-stage VCO, a frequency limiter RC circuit, and a ratioed VCO controlling current mirror. The targeted frequency is 500 MHz, while the output clock is ranged between 380 MHz and

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600 MHz. The fast lock time is 95 us in the worst case. The entire design is implemented by TSMC (Taiwan Semiconductor Manufacturing Company) 0.6 um lP3M CMOS technology and verified by HSPICE.

2. VCO DESIGN FOR LOW-JITTER PLL

As shown in Figure 1, the entire PLL circuits consists of a PFD (phase-freq detector), a charge pump, a second order loop filter, a VCO and a digital divider. In our design, the reference input clock is given 20 MHz which can be easily produced by most of the commercial crystal oscillators.

2.1. Frequency Limiter

Most of the PLLs are designed specifically for certain pre-determined operating frequency. Thus there is no need to sacrifice the lock time for the working frequency range from 0 MHz to a desired upper bound. Hence, we introduce a practical frequency limiter between the charge pump and the current mirror for ring oscillator in the VCO. The detailed frequency limiter is shown in Figure 2. We tend to take advantage of the W/L ratio of NMOS M2 to clamp the output frequency range and the upper bound of this range such that the actually highest frequency of the PLL is not the same as that of the ring OSC. Besides, this highest output frequency of the output frequency range can be determined by adjusting the resistance of $R1$ in Figure 2.

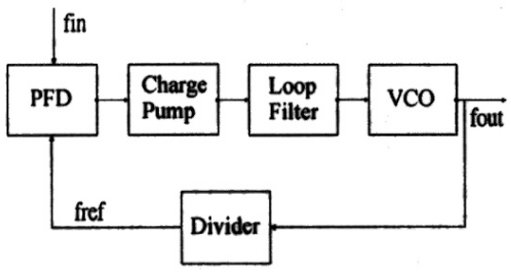

FIGURE 1 Block diagram of PLL.

In contrast, M3 itself can be deemed as a nonlinear RC circuit which is able to control the lowest output operating frequency. The smaller the W/L of M3, the lower the output frequency is. However, the ring OSC will not function if the W/L of M3 is smaller than a certain value. The size of M3 is thus used as an adjustable mechanism to determine the range of the output frequency. Another major benefit of such a circuit is to reduce the noise coupling effect of power supply to the ring OSC besides the mentioned frequency limiting function.

2.2. Load-optimized Ring OSC

Conventionally the ring OSC of the VCO used in high frequency PLLs is composed of three cascaded inverters with equal size. The might lead to a problem if the output of the VCO is connected to a buffer. It indicates that the last stage of the OSC possesses two loads while the other stages have only one. If the buffer size is sufficiently large in order to drive large load, the output of the VCO will damp to a stable voltage value if V in of the frequency limiter is small. Hence, we adopt a ratioed design for the cascaded inverters to optimize the loading at each stage. The sizes of the transistors used in the OSC are shown in Figure 2.

2.3. Fast Lock Time Consideration and Compensation

The mentioned frequency limiter basically provides an almost pre-determined bias voltage at the input of the VCO. Referring to Figure 3, the V-f diagram of the proposed VCO reveals that our design strictly focuses the targeted range, 500 MHz. The lock time will be drastically reduced owing to the none-zero output frequency given the lowest input voltage to the VCO. However, the drawback of the narrow band effect can be compensated by the digital frequency divider shown in Figure 1.

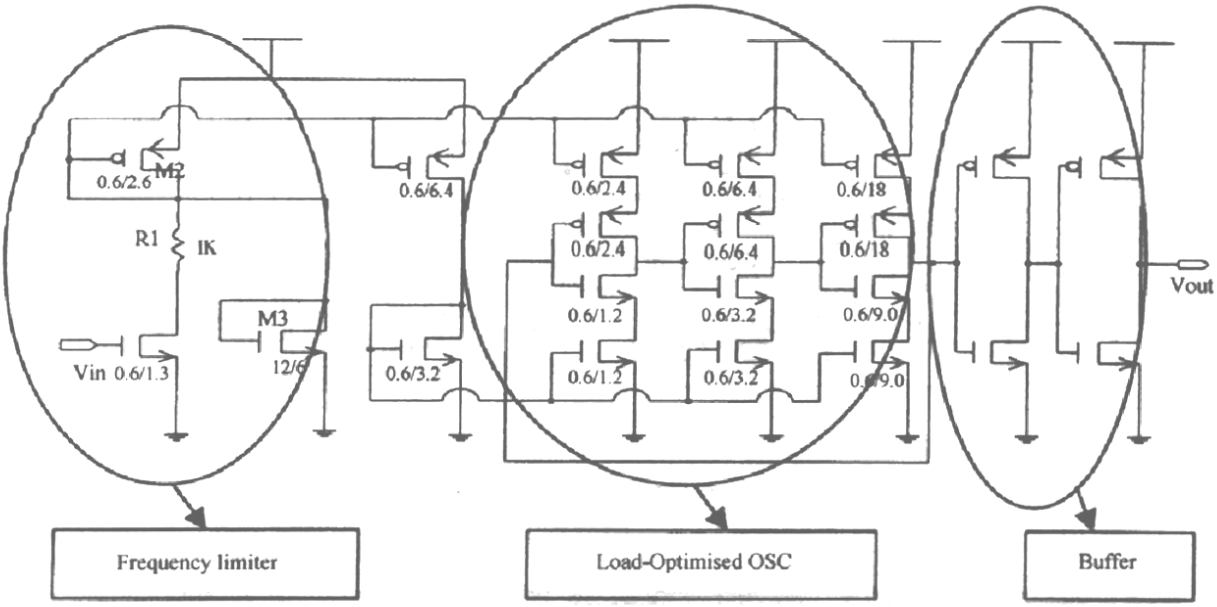

FIGURE 2 Schematic of the entire PLL.

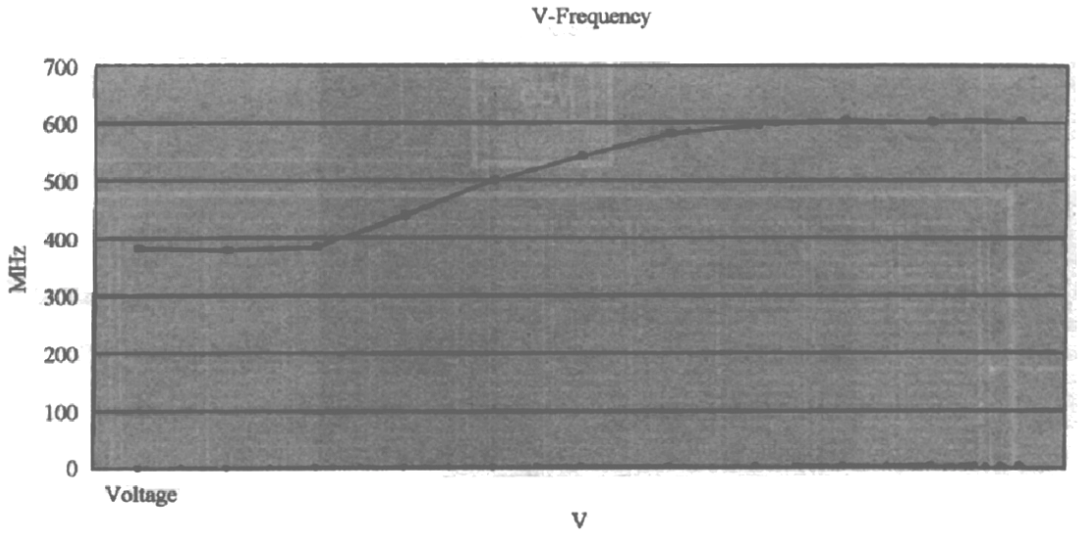

FIGURE 3 Schematic of the propose VCO.

3. SIMULATION RESULTS AND CHIP LAYOUT

To verify the correctness and functionality of the proposed design, we design the entire PLL circuit using TSMC 0.6 um 1P3M CMOS technology. The schematic and the layout are respectively shown in Figures 4 and 5. The capacitors in the loop filter are composed of gate-to-bulk capacitors of 50 parallel NMOS transistors, respectively.

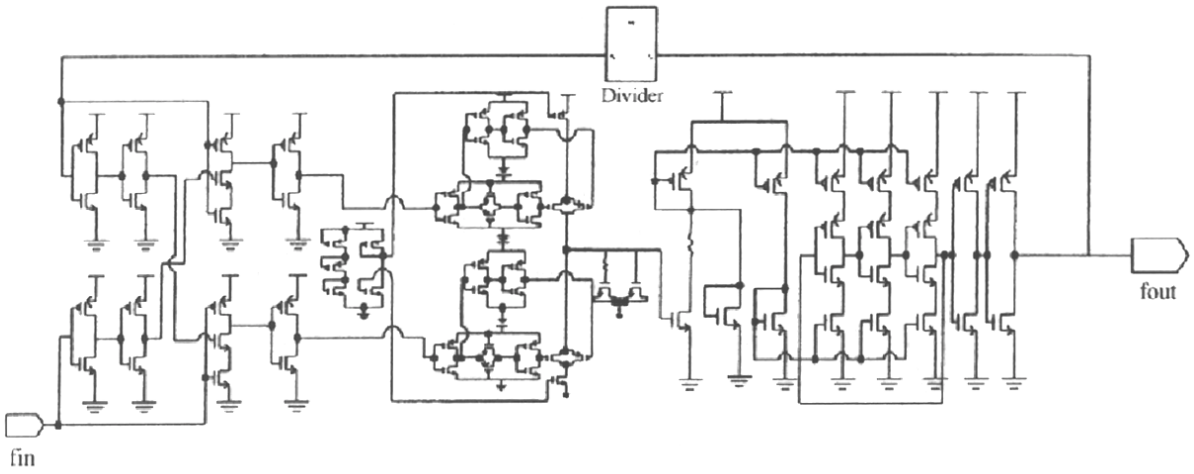

FIGURE 4 V-f diagram of VCO.

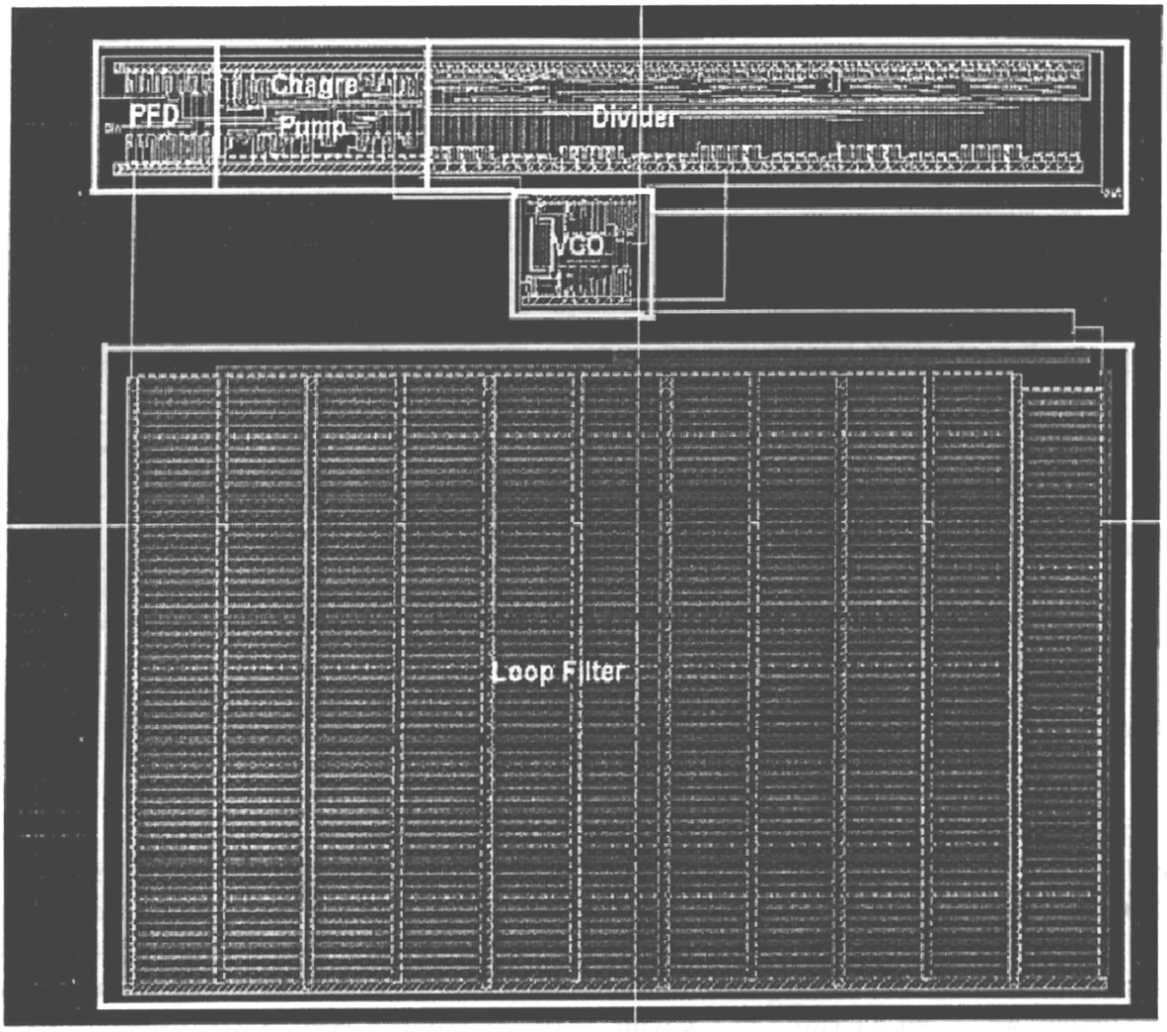

FIGURE 5 Gain-bandwidth of the loop filter.

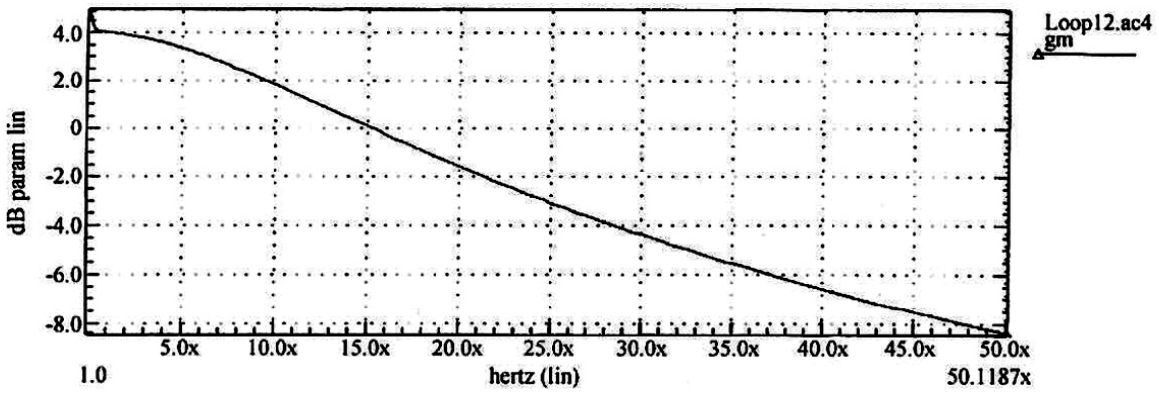

FIGURE 6 Layout of the propose PLL.

TABLE I Cycle-to-cycle VCO jitter at 600 MHz @5V 0.6 um 1P3M CMOS

jitter without supply noise	± 21.023ps
jitter given noise of 0.5V 1 MHz square wave	−70.6/+72.693ps
Sensitivity	286.6ps/V

TABLE II Jitter comparison without noise presence

	Lock time	Jitter	Lock freq.	Technology
[4]	N/A	80 ps	250 MHz	0.5 um CMOS 3V
[5]	N/A	144 ps	250 MHz	0.5 um CMOS 3.3V
[8]	N/A	81 ps	130 MHz	0.8 um CMOS 5V
Ours	43u	160 ps	480 MHz	0.6 um CMOS 5V

TABLE III Jitter comparison with noise presence

	Jitter p-p(ps)	Std. (ps)	Noise-level(v)	Sensitivity ps/V	Freq. (MHz)	Technology
[1]	133	20.97	0.5	N/A	360	0.5 um CMOS 3.3V
Ours	−70.6/+72.7	52.2	0.5	286.6	480	0.6 um CMOS 5V

That is, the source and drain of these transistors are all grounded. The gain-bandwidth diagram is given in Figure 6.

The measured sensitivity and the jitter performance is summarized in Table I.

The comparison of our design and prior works are also illustrated in the following Tables II and III.

Basing on the above results, the proposed design is superior to the prior works regarding the jitter and lock time.

TABLE IV Jitter measured by IMS200, which introduces about 0.2V power noise

Lock freq. (MHz)	Jitter (ps)	Std. (ps)
266.64	48	8.213
300.00	54	9.076
328.80	80	11.05
360.96	111	16.84
390.24	150	23.71
420.96	100	15.40
452.88	80	12.79
466.08	70	2.110

4. REAL CHIP TESTING RESULT

Ours design has been fabricated by TSMC and sponsored by CIC (Chip Implementation Center) of NSC (National Science Council). The chip no. is T06-88B-15. The testing equipment and environment are as follows: the power supply and the input clock are produced by ATM's IMS200, which introduces about 0.2 V power noise. The output frequency is measured by a oscilloscope. The room temperature is about 24°C. The total number of samples is 5,000. The real chip testing results are summarized in Tables IV and V, which respectively reveal the jitter measurement result and the operating frequency range.

TABLE V Frequency measured by IMS200, which introduces about 0.2V power noise

Lock freq. (MHz)	Mean freq. (MHz)	Max freq. (MHz)	Min freq. (MHz)	Std. freq. (MHz)
266.64	266.5	268.2	264.8	0.590
300.00	298.7	301.2	296.5	0.800
328.80	329.2	334.1	325.4	1.202
360.96	360.4	368.6	354.1	2.185
390.24	391.1	403.2	380.2	3.550
420.96	421.7	430.2	412.5	2.751
452.88	453.6	462.1	445.7	2.501
466.08	466.5	473.9	458.6	1.957

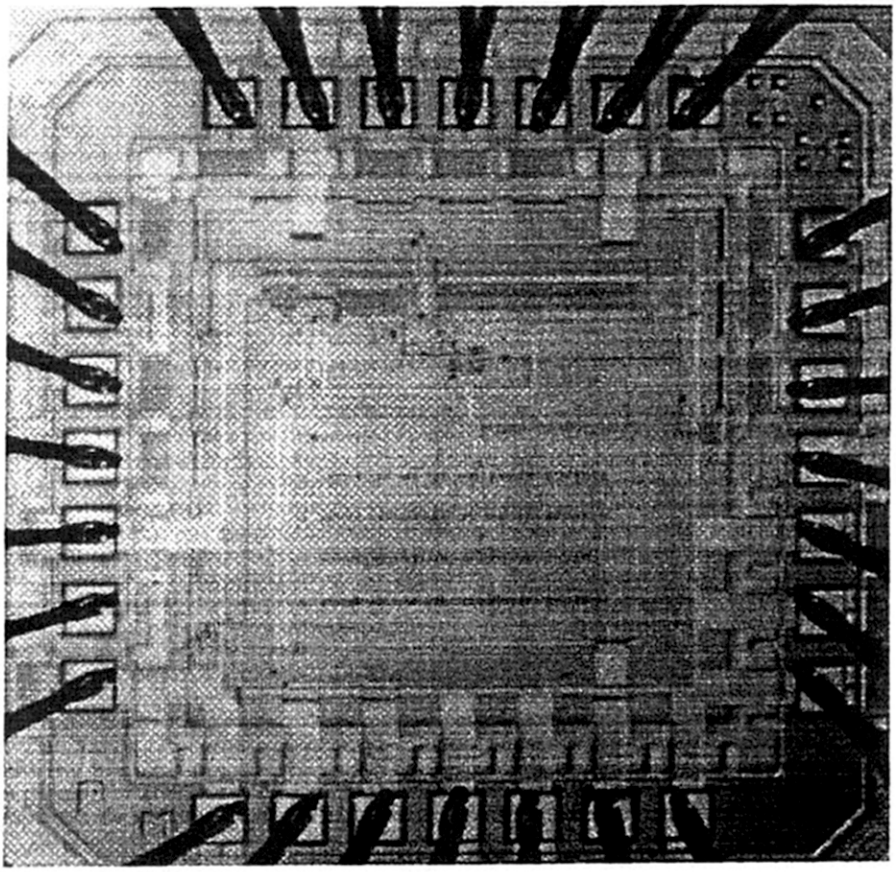

FIGURE 7 Die photo of our chip.

The die photo of the chip is shown in Figure 7. The locked frequency range of our real chip is between 266 MHz and 466 MHz which is a little lower than what we expected in Section 2.3 (500 MHz). The worse case of the jitter is 150ps, which is better than the simulation. There are two reasons why the performance of the real chip is better than the simulation. First, the significant digits of the simulation data are not long enough such that the precision is underestimated. Second, since the, frequency of the real chip is lower than the expectation value of the simulation results, a smaller jitter is then generated. Nevertheless, the real chip testing result is very close to the simulation results.

5. CONCLUSION

A novel and practical VCO design for digital PLL is presented in this paper. Besides shortening the lock time, the jitter caused by noise of the power supply is also reduced. Meanwhile, the loading effect of the ring OSC is taken into consideration. Simulation results provided by HSPICE reveal the value of the entire design. The performance of the real chip results show that our design is a practical approach.

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Authors' Biographies

Chua-Chin Wang was born in Taiwan in 1962. He received the B.S. degree in electrical engineering from National Taiwan University in 1984, and the M.S. and Ph.D. degree in electrical engineering from State University of New York in Stony Brook in 1988 and 1992, respectively. He is currently a Professor in the Department of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan. His recent research interests include low power and high speed logic circuit design, VLSI design, neural networks, and interfacing I/O circuits.

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