Single-Ended SRAM with High Test Coverage and Short Test Time

Chua-Chin Wang, Chi-Feng Wu, Rain-Ted Hwang, and Chia-Hsiung Kao

***Abstract*—The advantages of low power dissipation and smaller chip area for single-ended SRAM's are well known. In this paper, we present the configuration and test strategy of a single-ended, six-transistor SRAM. The benefits of short test time, no retention test, and high test coverage are verified. The goals of low power, high quality control, and short test time of the full CMOS SRAM can be achieved.**

***Index Terms*—High test coverage, IFA-9, retention fault, single-ended cell, SRAM.**

I. Introduction

One OF the major problems in SRAM testing is to obtain full fault coverage. As SRAM density becomes larger, the testing time will increase rapidly. Hence, the SRAM test cost occupies a significantly large portion of the total production cost. For future SRAM generations, the test cost is expected to rise even higher. Therefore, SRAM testing is becoming a challenging task in terms of quality and economics [1].

Because of two I/O sides in the SRAM cell, the structure of two-ended SRAM creates a lot of extra work during testing. When there is a defect at one end of the SRAM, the function of the other end can still compensate for it. Hence many fault models have been used to detect such a fault, e.g., the stuck-at fault (SAF), transition fault (TF), state-coupling fault (SCF), and data-retention fault. From the failure analysis results of [2], SCF and TF are mainly caused by the two-ended structure of the six-transistor SRAM.

Quiescent supply current (IDDQ) testing is one effective technique of detecting both bridge faults and open faults in CMOS integrated circuits. The open defects can be modeled by some stuck-at faults, whereas bridge defects cannot. Note that a defective circuit can still pass the functional testing and create risks in later field applications when the testing scheme depends on the resistance of the bridge faults [3], [4]. Nevertheless, the IDDQ test can detect the bridge faults, stuck-at faults, and break faults.

There have been attempts to use the IDDQ test method for detecting manufacturing process defects in SRAM's. Sachdev reported [1] that his design for SRAM IDDQ testing may not cover stuck-open faults in the matrix. Moreover, data-retention faults may not be covered by the IDDQ measurement. Thus, a combination of IDDQ and functional tests is necessary to achieve high-quality and low-cost SRAM testing.

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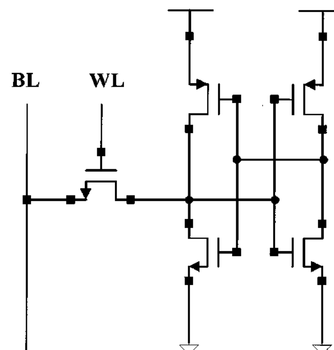

Fig. 1. Single-ended, five-transistor SRAM.

II. Circuit Design and Testability

A. Single-Bit-Line SRAM Cell

Fig. 1 shows a single-ended, five-transistor SRAM cell that can replace the basic six-transistor cell. The five-transistor SRAM cell contains one less device and one less bit line (BL) per cell than the common six-transistor cell. However, it has not been widely used because of lower operating margins and difficulty in performing the WRITE operation reliably with standard power supply. Restated, there is no problem with writing a "0," while writing a "1" is difficult since transferring data from the BL to the cell is a ratio-type operation. This makes the WRITE operation unreliable unless the word-line (WL) voltage is increased above the $V_{\rm DD}$ power supply. Thus, sophisticated control of peripheral units is required to ensure the reliability of the WRITE operation of the cell. This additional circuitry for the control might increase the chip area, thereby reducing the area-saving advantage given by such a memory cell design [5].

We propose a novel design by adding an NMOS write control transistor (WCT) in the cell, as shown in Fig. 2, and this WCT is controlled by the WRITE_. Thus, in the writing period, the big pulldown transistor of the cell no longer exists. However, because the input side of the cell is connected through a pass NMOS transistor, the high voltage can not reach full $V_{\rm dd}$. Hence, the threshold voltage of the first inverter has to be lower than 1/2 $V_{\rm dd}$ by adjusting the W/L ratios of the transistors. Besides, noise margins then will be kept.

To avoid disturbing the unselected cells during the WRITE operation, the WCT's are only opened for the columns of the selected word when the WRITE is high and the CLK is low. As for the unselected columns, the WCT's are closed to maintain the latch function. To optimize the speed, one might set the threshold voltage of the inverter, which is used as the sense amplifier, above 1/2 $V_{\rm DD}$ by adjusting the W/L ratios of the transistors. Fig. 3 is the schematic diagram of the proposed SRAM structure.

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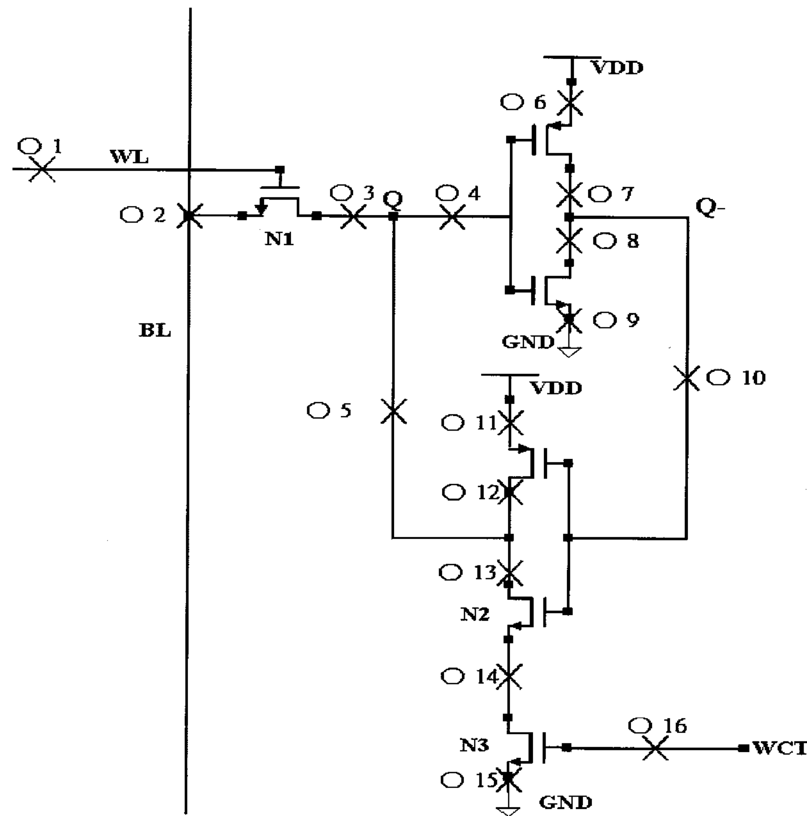

Fig. 2. Proposed single-ended, six-transistor SRAM and possible faults.

B. Test Strategy

The traditional IFA-9 scheme is shown as follows [2]:

$$\{\Updownarrow(\mathrm{w0});\ \Updownarrow(\mathrm{r0,\ w1});\ \Uparrow(\mathrm{r1,\ w0});\ \Downarrow(\mathrm{r0,\ w1});\ \Downarrow(\mathrm{r1,\ w0});\ \text{delay hundreds of ms};\ \Updownarrow(\mathrm{r0,\ w1});\ \text{delay hundreds of ms};\ \Updownarrow(\mathrm{r1})\}.$$

In contrast, the proposed test scheme for our SRAM is shown as follows:

$$\{\Updownarrow(\mathrm{w0});\ \mathrm{IDDQ};\ \Uparrow(\mathrm{r0,\ w1});\ \mathrm{IDDQ};\ \Uparrow(\mathrm{r1})\ \text{at predischarge};\ \Updownarrow(\text{w, checkerboard});\ \mathrm{IDDQ};\ (\text{r, checkerboard})\}.$$

Next we will discuss the proposed scheme.

1) $\Updownarrow$*(w0); IDDQ:* Short faults in the cell may cause SAF or IDDQ fault. If the resistance of the defect is low enough, then the SAF will be observed. The SAF is defined as follows. The logic value of a stuck-at (SA) cell or line is always "0" (an SA0 fault) or "1" (an SA1 fault); that is, it is always in state "0" or in state "1" and cannot be changed to the opposite state. If the resistance of the defect is high but still creates measurable static current, then the IDDQ fault will be observed. The open fault at the input of the inverter will cause floating-gate effect and poorly defined gate voltage; then a leakage path from V_{dd} to V_{ss} can be detected. This test is to detect the IDDQ when the cell content is zero. During this period, the BL are pulled up to V_{dd} and the content of the cell is zero. This IDDQ test can also detect the leakage between the source/drain of the pass transistors.
2) $\Uparrow$*(r0, w1):* This test is to detect stuck-at-1 (SA1) faults.
3) *IDDQ:* This test is to detect IDDQ faults when the cell retains "1."
4) $\Uparrow$*(r1) at predischarge:* The (r1) test is to detect stuck-at-0 (SA0) faults. The predischarge algorithm is to detect the retention faults without adding the delay time. The retention fault is caused by a broken pullup transistor. In a general precharge mode, the BL is precharged to V_{dd}, and then read "0" of the SRAM cell is decided by discharging the BL through the NMOS transistor of the cell. Because of the BL precharged to V_{dd}, a broken pullup transistor in the SRAM cell can still make the read "1" work properly. The retention time depends on the capacitance of the node and the leakage current from the defective node to V_{ss}. By contrast, in a predischarge mode, the BL is predischarged to V_{ss}, and then read "1" of the SRAM cell is decided by the pullup of the BL through the PMOS transistor of the cell. A broken pullup transistor in the SRAM cell will not be able to pull the BL up to read "1." Thus, no delay time is needed for the retention detection. However, we need a sense LOW amplifier in the normal operation with BL precharged, and we need a sense HIGH amplifier in the predischarge mode. Hence, the sense amplifier should be designed to switch between sensing LOW at the normal mode and sensing HIGH at the predischarge mode.
5) $\Updownarrow$*(w, checkerboard), IDDQ:* This test is to detect the IDDQ of SCF.

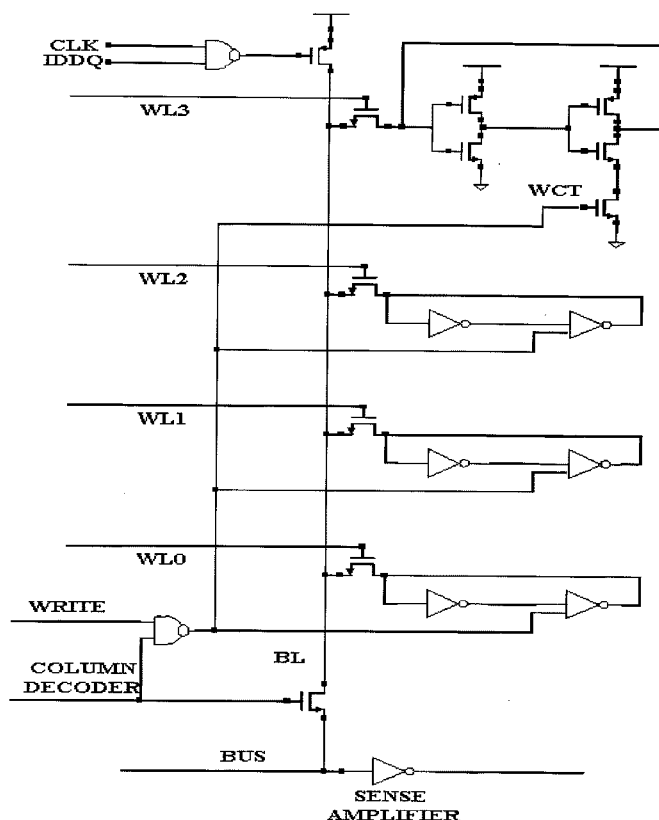

Fig. 3. Schematic diagram of the proposed SRAM.

TABLE I
POSSIBLE SHORT DEFECTS EXISTING IN FIG. 2

Short nodes	VDD & GND	VDD & VGND	VDD & WL	VDD & BL	VDD & Q	VDD & Q-	VDD & WCT	GND & VGND	GND & WL	GND & BL
Stuck-at Fault				Yes					Yes	Yes
IDDQ and/or SA Fault	IDDQ	Yes	Yes		Yes	Yes	Degr.	Degr.		
Short nodes	GND & Q	GND & Q-	GND & WCT	VGND & WL	VGND & BL	VGND & Q	VGND & Q-	VGND & WCT	WL & BL	WL & Q
Stuck-at Fault			Yes	Yes	Yes			Yes		
IDDQ and/or SA Fault	Yes	Yes				Yes	Yes		Yes	Yes
Short nodes	WL & Q-	WL & WCT	BL & Q	BL & Q-	BL & WCT	Q & Q-	Q & WCT	Q- & WCT		
Stuck-at Fault										
IDDQ and/or SA Fault	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes		

6) $\Updownarrow$*(r, checkerboard):* This test is to detect the SCF.

The detectable defects are shown in Tables I (short defects) and II (open defects) as in Fig. 2.

C. Area Overhead and Speed Penalty

The word-wise structure needs a NAND gate and buffers to control the WCT's of every word column. If we want to implement the predischarge algorithm, an extra NAND in every BL to control the precharge activities is required, as shown in Fig. 3. In addition, we need two NOR gates to control the precharge/predischarge of the data buses. In our design, the overheads are 128 + 16 NAND gates and 16 NOR gates with some buffers. If we do not use the predischarge algorithm, the overheads will be only 16 NAND gates with some buffers to control the WCT's.

TABLE II
POSSIBLE OPEN DEFECTS EXISTING IN FIG. 2

Open node	O1	O2	O3	O4	O5	O6	O7	O8	O9	O10	O11	O12	O13	O14	O15	O16
Stuck-at Fault		Yes	Yes		Yes	Yes	Yes	Yes	Yes		Yes	Yes	Yes	Yes	Yes	Degr
IDDQ and/or SA Fault	Yes			Yes						Yes						

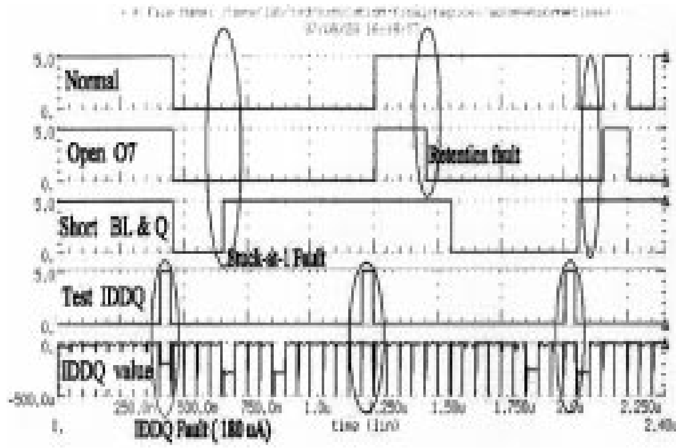

Fig. 4. Simulation waveforms: (a) normal output, (b) output of open fault O7, (c) output of short fault between BL and Q, (d) IDDQ test periods, and (e) IDDQ measure values.

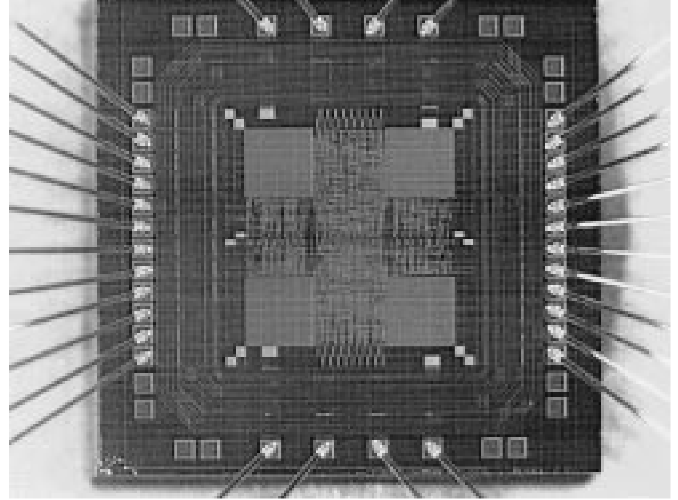

Fig. 5. The microphotograph of the experimental device with four 128 × 8 blocks of single-ended SRAM.

The read access time of the SRAM is decided by the discharge rate of the BL through N1, N2, and N3, which is proportional to a time constant as follows:

$$\tau \approx \frac{C_{\mathrm{BL}}}{K'\left(\frac{W}{L}\right)(V_{\mathrm{dd}} - V_t)^2} \times \Delta V \tag{1}$$

where C_{BL} is the total bit-line capacitance, K' is the intrinsic transconductance of N-transistor (μc_{ox}), W/L is the equivalent width-to-length ratio of the serial N1(0.9/0.6), N2(1.6/0.6), and N3(1.6/0.6), V_{dd} is the supply voltage, V_t is the N-transistor threshold voltage, and ΔV is the discharge voltage amount [7]. The added WCT in the discharge path will reduce the discharge speed. According to the above formula, which assumes that the transistors are in the saturation mode, there will be a 36% speed loss with the mentioned transistor sizes when compared with the traditional six-transistor SRAM. From the HSPICE simulation, the speed penalty is about 22% with the benefit of about 40% power saving. The speed loss can be improved by enlarging the size of N3. If we consider the discharge of the data bus capacitor, which is discharged through the pass transistor controlled by the column decoder, the speed loss will be less than the previous estimation.

III. SIMULATIONS AND EXPERIMENTS

To verify the proposed strategy, we conducted a series of the simulations by using TSMC 0.6-μm 1P3M CMOS process for 5-V operation. All of the faults listed in Tables I and II are simulated by HSPICE. The open defect is simulated with a 100-GΩ resistance. It is verified that any existing resistive path (5000 Ω) is either IDDQ or SAF detectable besides the short between the source/drain of the WCT. The open fault at the input of the inverter will cause floating-gate effect, but it is not so easy to simulate the leakage current caused by open faults. However, the open faults can be detectable by the function tests. For retention faults caused by the open defects on the pullup transistors, owing to the single-ended structure, one of the retention faults will be changed to SAF, and the second retention fault can be detectable when the predischarge of BL is used during this test period. Some of the simulation waveforms are shown in Fig. 4.

Regarding the short between the source and drain of the WCT, the purpose of WCT is to aid the "WRITE one" operation. If the WCT is stuck on, the "WRITE one" operation will be degraded at high frequency and stuck at zero, depending on the ratios of the transistors. As the open at the gate of the WCT, it may cause SAF, or the operation frequency will be degraded and the fault can be detected at high frequency, depending on the state of the floating gate.

According to the results of the HSPICE simulation, our test scheme makes the test of the single-ended SRAM easily implemented to detect bridge, open, and retention faults.

IV. CIRCUIT IMPLEMENTATION AND TESTING

A. Circuit Implementation

To demonstrate the proposed ideas on silicon, we designed a 512 × 8 single-ended SRAM by using the same TSMC 0.6-μm 1P3M CMOS process used for the schematic simulation. The single cell size is 128 μm2. The chip is successfully fabricated.

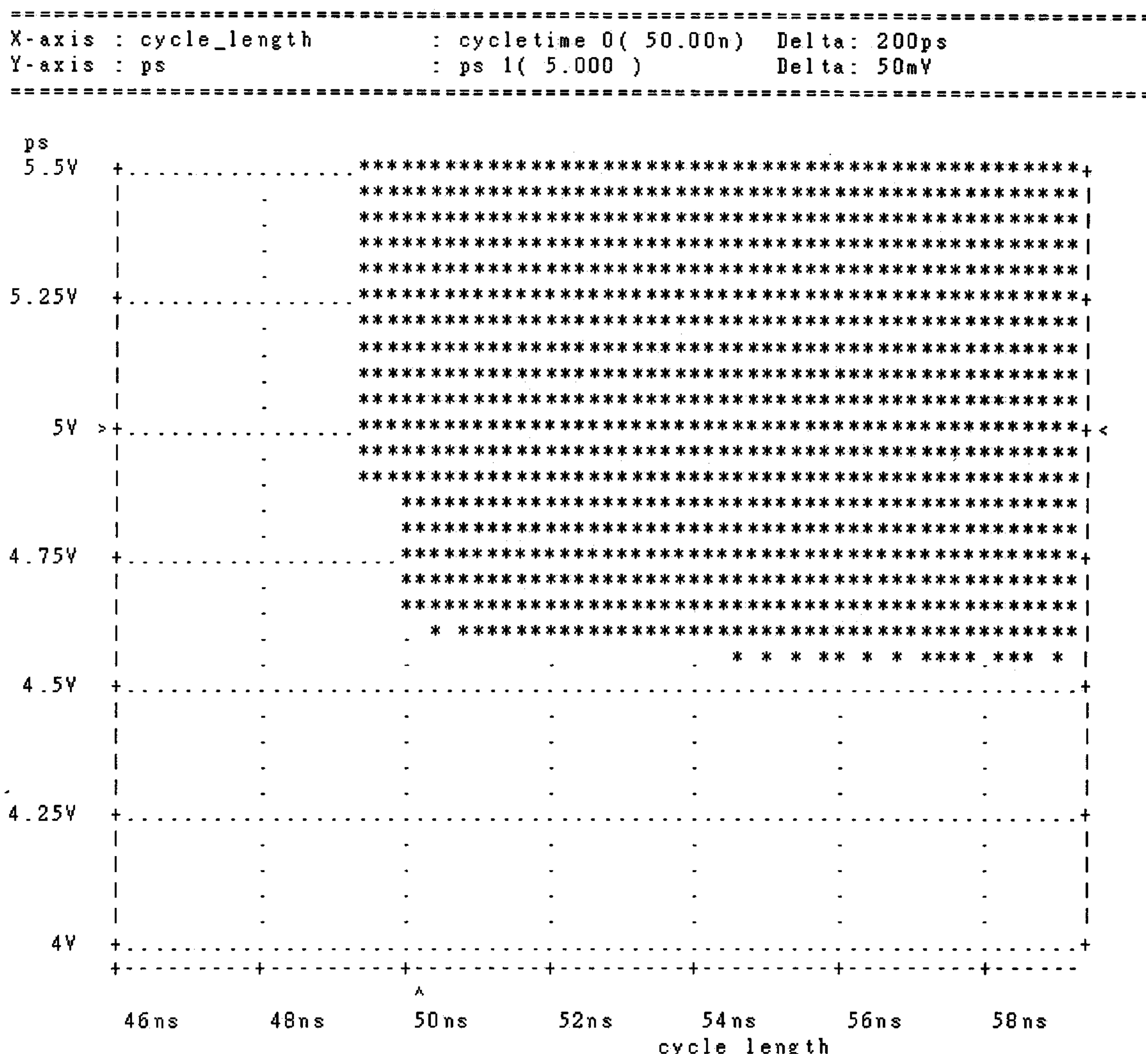

Fig. 6. The shmoo of $V_{\rm dd}$ versus cycle length of the proposed single-ended SRAM.

Fig. 5 shows the microphotograph of the experimental device. The cell array is divided into four 128×8 blocks.

B. On Silicon Faults Generation and Testing

To verify the function of the device, we used the *Credence VistaVision* automatic test equipment to test the functionality of the device. The typical standby current of this chip is about 6 nA. The operation current is 6.69 mA at 10 MHz of looping $\Downarrow$(w1); $\Downarrow$(r1, w0); $\Downarrow$(r0). The shmoo of the proposed single-ended SRAM is shown in Fig. 6.

In order to generate all of the possible faults, we use a focused ion beam (FIB) to create the possible open and short faults on the functional chip. The FIB is equipment that is usually used for circuit modification and failure analysis of IC's [6]. The detectabilities of the generated faults are verified.

V. Conclusion

A six-transistor, single-ended CMOS SRAM structure and its test scheme are proposed. Because only the single bit line needs charging and discharging during operation, the single-ended SRAM can reduce the power consumption dramatically. In addition, the single-ended structure will reduce the complexity of the RAM cell, thus simplifying the possible fault models. The transition fault and one of the retention faults will be changed into SAF's. With the predischarge then read algorithm, the second retention fault can also be changed to SAF. Thus, the test complexity is reduced. The benefits of low power, short test time, and high test coverage of the proposed design are verified on silicon. The goals of low power, high quality control, and short test time of full CMOS SRAM are achieved.

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