Experimental results and conclusions: To demonstrate the effectiveness of the proposed layout scheme, we experimented with several examples from a 64bit real microprocessor design. For the 64bit datapath having 15 tracks for each bit slice, the interconnect length for the control wire becomes 1000μm, and the width and spacing are selected to be the minimum size in a 0.25μm CMOS process. Table 1 shows the experimental results on several circuits consisting of 3-to-1 and 4-to-1 multiplexers with different transistor size and interconnect RC. On average, the multiplexer delay is improved by 14.3% and the average current is reduced by 9.6%.

Change of selection from i to j (i->j): 1->2 1->3 1->4 2->1 2->3 2->4 3->1 3->2 3->4 4->1 4->2 4->3 — total opposite transitions: *a* 24, *b* 12, *c* 0

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Fig. 2 *Switching direction of selection control signals for each case of control signal transition in 4-to-1 multiplexer*

a Scheme 1
b Scheme 2
c Proposed scheme
Dotted boxes show worst-case transitions

Table 1: Effect of control signal layout ordering scheme on delay and average current

Example	Scheme 1		Proposed		Improvement [%]	
	Delay	Current	Delay	Current	Delay	Power
	ps	mA	ps	mA	ps	mA
ex0	486	147.489	433	136.212	10.84	9.94
ex1	526	155.603	453	140.141	13.78	7.65
ex2	502	75.037	421	66.239	16.14	11.72
ex3	614	93.713	531	86.332	13.52	7.88
ex4	652	161.42	579	153.33	11.20	5.00
ex5	527	72.201	425	62.8421	19.39	12.96
ex6	503	73.039	414	64.128	17.69	12.13
ex7	546	92.013	474	83.194	13.29	9.58
ex8	538	93.673	469	84.713	12.79	9.57
Average					14.3%	9.6%

To mitigate the cross-coupling effect, the signal switching in the opposite direction should be suppressed for the control signals in the datapath. In this Letter, we have proposed an interconnect layout scheme for minimising the cross-coupling effect. The new signal ordering scheme was shown to reduce the power consumption by 10% and the delay by 15% for a given set of experimental benchmarks based on 0.25μm DSM technology.

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In-sawing-lane multi-level BIST for known good dies of LCD drivers

Chua-Chin Wang, Chi-Feng Wu, Sheng-Hua Chen and Chia-Hsiung Kao

Liquid crystal display (LCD) drivers usually operate at low speed, and have a low input-count but high output-count with multi-level voltages. A novel built-in-self-test (BIST) method for LCD drivers is proposed to reduce testing costs. This BIST circuit will be placed in the sawing lanes to reduce the chip area. The chip overhead and the testing costs are reduced, while the test coverage can be maintained.

Introduction: In traditional litho-technology, a drop-in process control module (PCM) is used to measure the parameters for process control. To improve the steppers' efficiency, sawing-lane PCMs have been widely introduced to replace drop-in PCMs with a lane width of ~150μm. Since the sawing lanes consume wafer area, the potential number of good dies per wafer (PGDW) will increase as the lane width decreases. For example, ~6% of the wafer area of a 25mm^2 chip is used for the sawing lanes. This is more severe for smaller chips. For example, ~10% of the wafer area of a 9mm^2 chip is used for the sawing lanes. To improve the PGDW, it is important either to make good use of the sawing lanes or to reduce the sawing lane width.

In design for testability, usually > 5% of the chip area is occupied by the test circuits, which are of no use for the normal operation of the chip. The known good dies (KGD) approach is becoming more and more popular for reducing the packaging size and weight of a complete system. In the KGD approach, the chips will be sent to customers for system assembly after the wafer testing without any packaging. Therefore, there is no chance for final testing. Thus, the test circuits in the chip are useless after wafer testing.

General-purpose high pin-count (and concomitantly high speed and high price) automatic test equipment (ATE) is usually used to test LCD drivers. This increases the testing cost of LCD drivers. In this Letter, we propose a BIST circuit for a multi-level LCD driver output. We also propose the insertion of this BIST circuit in the sawing lanes to reduce the total chip area. Thus, the testing cost is reduced and the area penalty of the test circuits minimised. A test circuit can be shared by neighbouring chips so as to make the test circuit more efficient. For example, when the left chip of the test circuit is tested, the outputs of its right chip are tri-stated, and vice versa. A control circuit for performing this function can be realised with three pins, V_{dd}, V_{ss} and a tri-state control signal.

Design of multi-level BIST: Because most of an LCD driver's pins are outputs, a comparison function is adequate. The expected data for the entire test can be compressed and compared by a signature analyser. The signature analysis involves a compression technique based on cyclic redundancy checking (CRC) by using linear feedback shift registers (LFSRs) [2].

Another problem to be resolved is how to handle the multi-level voltage of the LCD driver outputs. The digital system and the signature analyser can only process the results of '0' or '1'. An 8bit

ADC, which might be available in the LCD, is used to convert the multi-level signal into a digital signal. The bit count of the ADC depends on the number of biasing levels and the allowed tolerance of the biasing voltages. The LCD driver with a biasing voltage within the tolerance of the given specification should be treated as a pass device. Take the Philips' type PCF2103 as an illustrative example [3]. We use an 8 bit to 3 bit encoder to discriminate the tolerance of each voltage level. The encoding results with tolerance are shown in Table 1.

Table 1: Encoding of LCD driver outputs

Ideal value of LCD after ACD (decimal)	Acceptable value after ADC (decimal)	Encoded signals (binary)
0	0–5	000
63	58–68	001
84	79–89	010
127	122–132	011
170	165–175	100
191	186–196	101
255	250–255	110
others	fail	111

A multi-input signature analyser (MISR) [4] following the encoder circuit, which will be placed in the sawing lane, compresses the output signals to generate the signature. After test vectors are fed in, the MISR will generate a pass/fail signal. The pass/fail signals are then compared. The same procedure is executed until all the LCD outputs have been tested.

Layout notification for BIST: During the sawing process, the BIST circuits will be cut-through. To prevent the influences of these cut-through circuits on the functional area, two issues have to be addressed to ensure good isolation between the function area and BIST circuits after sawing:

(i) The connection between the power lines of the functional circuits and the BIST circuits must be cut in order to isolate the power of the BIST circuits. Otherwise, a leakage current may flow from the power lines of the functional circuits through the cut devices.

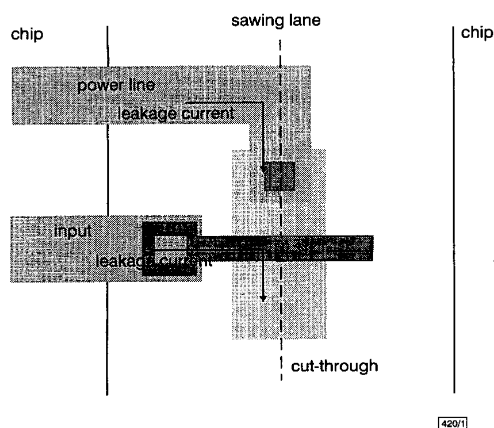

Fig. 1 *Layout in BIST with potential leakage problem after sawing*

(ii) The connection between the outputs of the functional circuits and the BIST circuits must be cut. Otherwise, a leakage current could flow from the outputs of the previous stage to the damaged transistors. In short, any path has to cross the central line of the sawing lane before being connected to the BIST circuits to ensure a good cut and isolation after sawing. Also, it would not consume extra area in a multi-metal process technology. Fig. 1 shows a problematic layout in the BIST after sawing. Fig. 2 shows a layout in the BIST with good isolation after sawing.

Simulation and testing: To implement the mentioned testing methodology, we designed an ASIC chip composed of an 8-to-3 encoder followed by a 32 bit MISR as the next stage of the A-to-D conversion. The design was written by synthesisable Verilog RTL codes, which were then synthesised by SYNOPSYS into gate-level circuits with a COMPASS cell library. The proposed multi-level BIST circuit was fabricated in a TSMC 0.6μm 1P3M process with a chip area of 0.54mm^2. The circuit can operate correctly over a 100MHz clock rate. With a lane width of 100μm, we need to fill 5.4mm length in this BIST circuit. Since the LCD proto-chip consumes an area of ~2 × 12mm^2 with a high aspect ratio, this BIST circuit is small enough to be placed in the sawing lane.

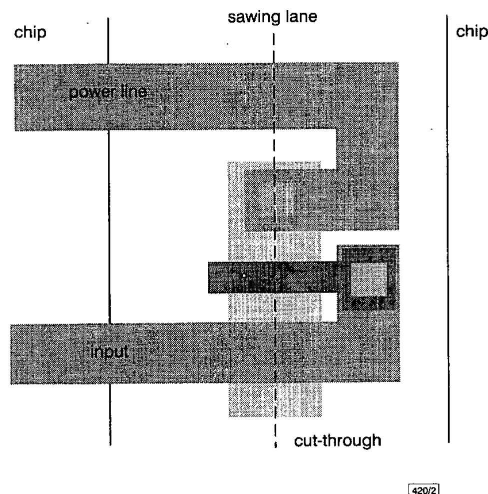

Fig. 2 *Layout in BIST with good isolation after sawing*

Conclusions: We have collected statistics for the chip areas of ~400 consumer products. The chip areas of 60% of those products are < 25mm^2. This means > 6% the wafer area is used for the sawing lanes for those products. The test circuits can be placed in the sawing lanes to reduce the area overhead due to design for testability (DFT) requirements.

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