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Dynamic NOR-NOR PLA design with IDDQ testability

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Certain logic functions such as the control units of VLSI processors are difficult to be implemented by random logic. Since the programmable logic arrays (PLAs) can implement almost any Boolean function, they have become popular devices in the realization of both combinational and sequential circuits. Besides, due to high quality demand in the semiconductor market, the testing of PLAs becomes an important issue. Because the structure of the PLAs is basically arrays of transistors or gates, the traditional test generation algorithms for stuck-at faults are hard to be employed. Thus, many test-generation approaches and designs for PLA testability have been developed. The IDDQ test is one of the effective techniques of detecting both bridge faults and open faults in CMOS integrated circuits. We present a testability configuration of PLAs which will be transformed into inverters in the test mode so that the IDDQ testing with only two test vectors and low overhead circuitry for the detection of all the bridge faults and most of the open faults can be realized.

1. Introduction

A PLA consists of three parts: an input decoder, an AND plane and an OR plane. PLAs can be implemented by either static or dynamic styles. The style is chosen depending on the timing strategy. For the purposes of high speed, low power (Wang and Jeng 1995) and small area, a dynamic CMOS NOR-NOR PLA is often used (Linz 1991, Blair 1992). Because of the PLA's structure, a new class of fault, known as cross point faults, often occurs. Four kinds of cross point fault have been defined in Abramovici *et al.* (1990): shrinkage fault, growth fault, appearance fault, and disappearance fault. These faults usually occur during the fabrication, e.g. bridge faults of metal bridge, gate oxide leakage, junction leakage, parasitic transistor leakage and open faults of metal broken, blind contact to source-drain and blind via, etc. The open faults can be modelled by some stuck-at faults. However, the bridge faults cannot be modelled by stuck-at faults. Note that a defective circuit can still pass the function testing but it creates risks in the later field application when the testing scheme depends on the resistance of the bridge faults (Wallquist 1995).

2. Transformation for IDDQ testing mode

It is well known that most defects in CMOS circuits can be divided into opens and shorts (Sachdev 1995). IDDQ testing is one of the effective techniques for detecting both bridge faults and open faults in CMOS integrated circuits. However, the controllability in CMOS circuits makes it harder to detect all the faults for IDDQ testing. Usually a number of test vectors are required to drive the circuits

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into proper states so as to achieve high test coverage. Therefore, the simplicity of the controllability condition becomes an important issue for IDDQ testing.

2.1. *Transformation of PLAs for detection of faults*

For an inverter, two vectors are enough to detect all of the possible faults, including shorts and opens (Wu *et al.* 1997). Hence, a simple thought is that by adding a control transistor in every product line and output line of the NOR-NOR style PLA, as shown in figure 1, we can control the state at the output of every node.

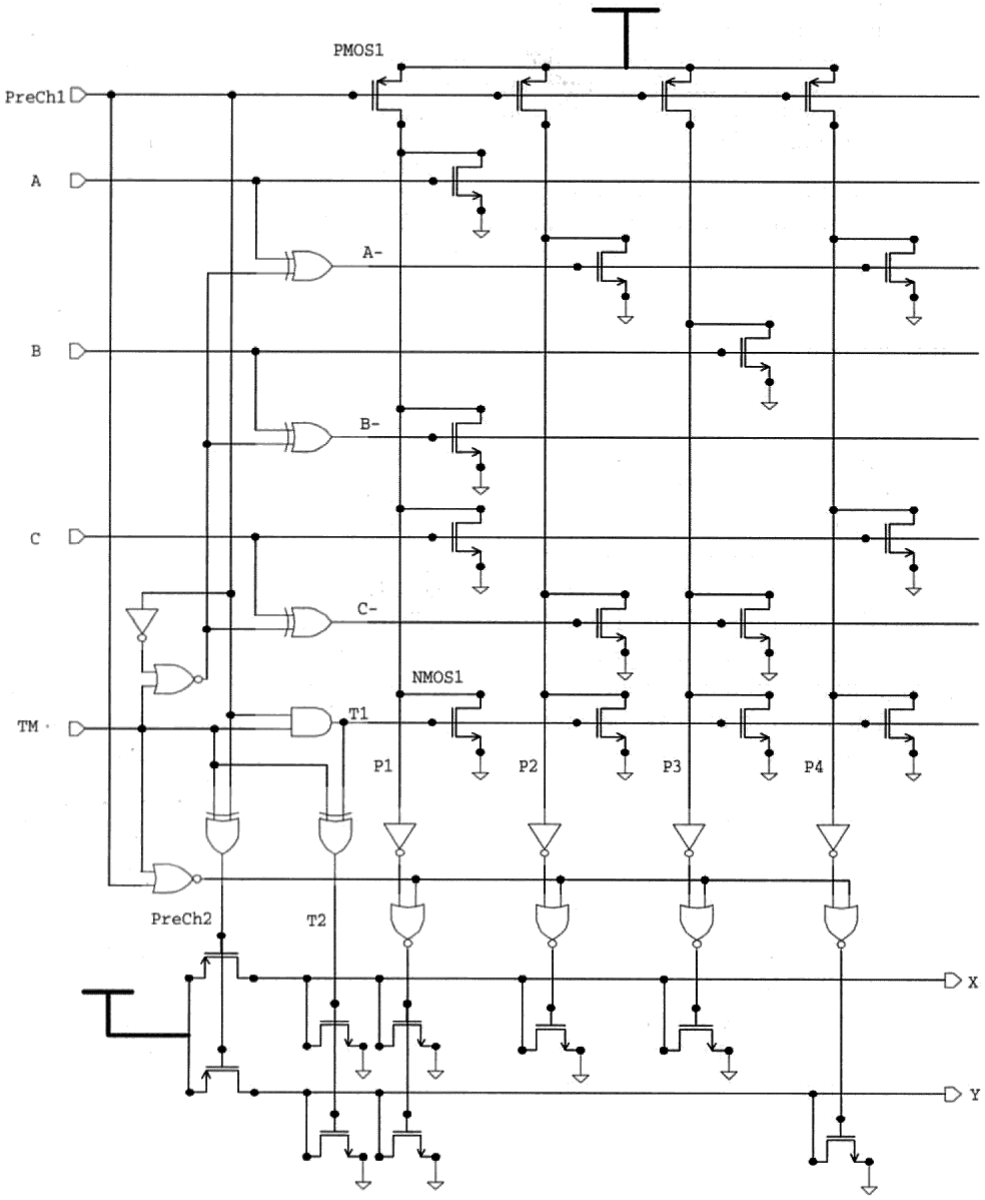


Figure 1. Schematic of the proposed PLA design.

Then the IDDQ testing of the PLA circuits can be treated as the IDDQ testing of combinations of inverters when the state of the inserted control transistor is appropriately assigned. The details are discussed as follows.

2.1.1. *The short detection for precharge PMOSs and the evaluation blocks.* Because the states of every product line can be controlled by the signals of PreChx and Tx, the shorts between adjacent product lines or output lines will be IDDQ detectable by assigning the states of each pair of neighbouring output lines differently from each other. Besides, since every node is controllable, we can set it high and then low. Thus any short-circuit defects of transistors can be detectable.

In the test mode (TM=H), the XORs of the input lines work like buffers. The PreCh1, T1 and all of the inputs are set to high. Thus the PMOSs and the NMOSs of the first NOR plane are turned off and on, respectively. Then the leakage of DG, DS and DB of PMOSs, and the leakage of DG, GS and GB of NMOSs will be detected. Meanwhile, PreCh2, T2 and all of the inputs of the second NOR plane are low. Thus, the PMOSs and the NMOSs of the second NOR plane are turned on and off, respectively. The leakage of DG, GS and GB of PMOSs of the second NOR plane, and the leakage of DG, DS and DB of the NMOSs of the second NOR plane can be detected.

In contrast, we can set the PreChl, T1 and all of the input bit-lines low in the test mode (TM=H). Then the PMOSs and the NMOSs of the frst NOR plane are turned on and off, respectively. Then the leakage of DG, GS and GB of PMOSs, and the leakage of DG, DS and DB of NMOSs will be detected. At the same time, PreCh2, T2 and all of the inputs of the second NOR plane are set to high. Thus, the PMOSs and the NMOSs of the second NOR plane are turned off and on, respectively. The leakage of DG, DS and DB of PMOSs of the second NOR plane, and the leakage of DG, GS and GB of the NMOSs of the second NOR plane can be detected.

In short, the vectors in the test mode and the corresponding detected nodes are summarized in Table 1.

2.1.2. *Gate open detection.* It has been reported that open defects leading to floating gates can also be detected if the gate acquires a sufficient voltage to leak current (Singh *et al.* 1995). This technique, which can detect the leakage current of open faults by liquid crystal analysis and light emission microscope, is also widely used in the practical failure analysis of CMOS integrated circuits. In Singh *et al.* (1995), IDDQ testing with random vectors detected 48 out of 59 open defects. In PLA blocks, all of the NMOS are parallel and are connected together to a precharge PMOS. As long as the PMOS is turned on, which can be controlled by the precharge signal, and the gate of NMOS is floating, the leakage current will be measurable.

Vector	TM	PreCh 1	Other I/Ps	Faults to be detected in the 1st NOR	Faults to be detected in the 2nd NOR
1	H	H	H	PMOSs' DG, DS and DB NMOSs' DG, GS and GB	PMOSs' DG, GS and GB NMOSs' DG, DS and DB
2	H	L	L	PMOSs' DG, GS and GB NMOSs' DG, DS and DB	PMOSs' DG, DS and DB NMOSs' DG, GS and GB

Table 1. The testing vectors and the corresponding detectable nodes.

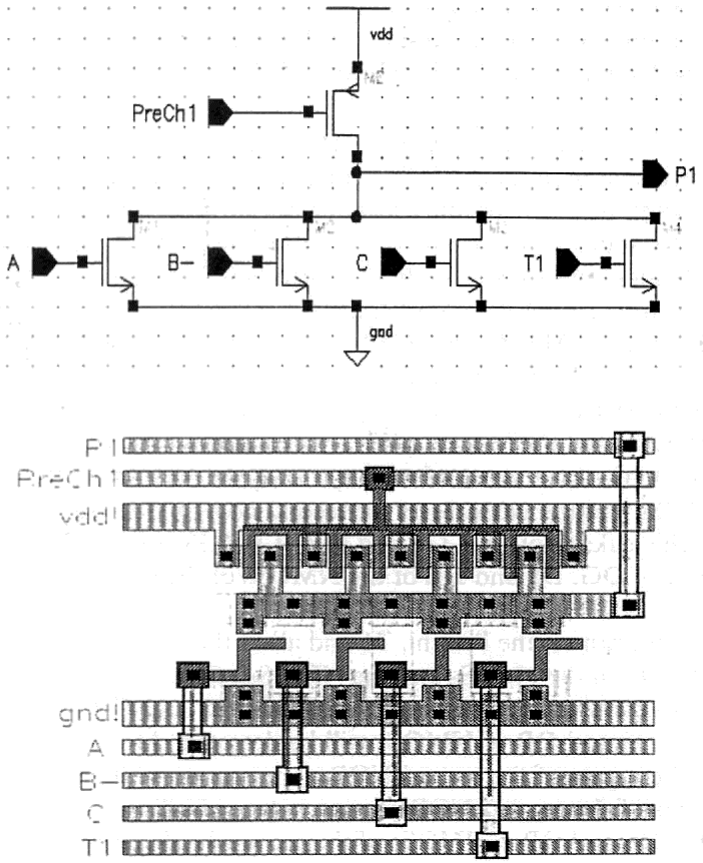


Figure 2. Schematic and layout of the test transistor for open faults.

2.1.3. *Source/drain open detection.* A source/drain open will introduce a floating gate in the next input circuit and then induce leakage current. With a special layout as in figure 2, we can make the source/drain of the test transistor open when any open happens in the product line or output line of the PLA. Then the open fault can be easily detected. Moreover, faults that are not detected usually behave like stuck-at faults and can be reliably detected by Boolean testing.

2.2. *Overhead analysis*

For an $n \times m \times k$ PLA, the overhead of the proposed testability design is listed as follows:

(1) ($m + k$ NMOS transistors): The test transistor for every product line and every output line for an $m \times k$ PLA.

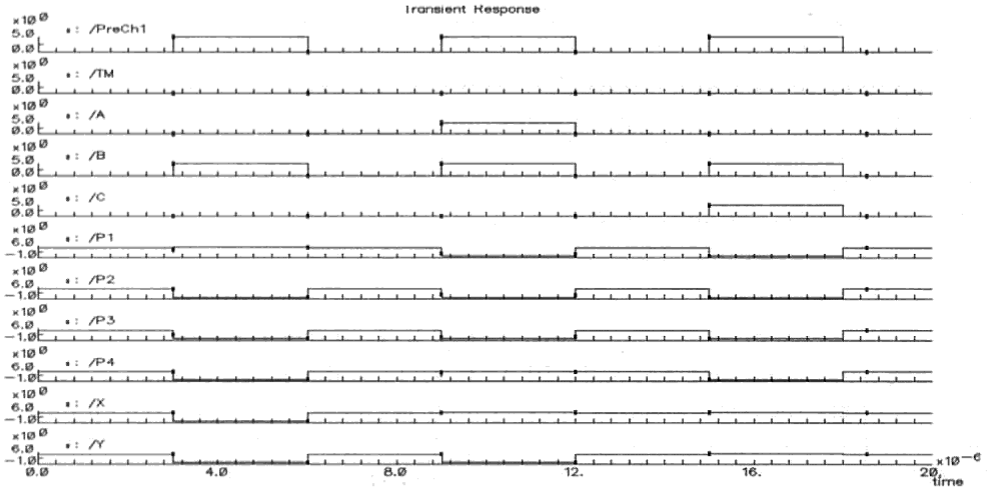
(2) n XORs (two NMOSs and two PMOSs, because [6 transistors of a XOR − 2 transistors of an inverter]): XOR is used to replace the inverter for every input line. In the evaluation period of the normal mode, it works as an inverter. In the test mode and the discharge period of normal mode, it works as a buffer in figure 1.

(3) Two XORs (three NMOSs and three PMOSs, because transmission gate type XORs are used (Wang *et al.* 1994)): To control the PreChx and Tx signals as shown in figure 1.

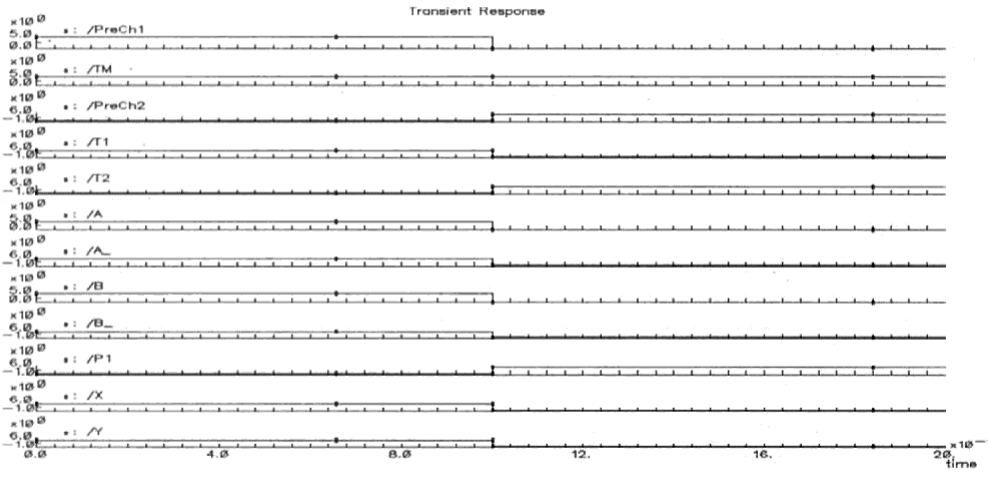
(4) One inverter, two NORs (two NMOSs and two PMOSs) and one AND (three NMOSs and three PMOSs)

(5) m NORs (one NMOS and one PMOS, because [4 transistors of a NOR $-$ 2 transistors of an inverter].)

Hence, the total overhead transistor count: $(m+k)+4n+12+16+2m$. Note that n, m, and k are the number of inputs, product lines and outputs of the PLA. The total cost is much less than that of other designs for PLA testability, e.g. Abramovici *et al.* (1990).



(a) Normal mode



(b) Test mode

Figure 3. Simulation waveforms of the proposed PLA in normal mode and test mode.

Circuit under test	Average current
No fault	0.2062 nA
Short S-D of NMOS1 (50 kΩ)	0.9714 mA
Short S-D of PMOS1 (50 kΩ)	0.9952 mA

Table 2. The power dissipation comparison of faulty and fault-free PLAs.

3. Simulation and analysis

In order to verify the proposed IDDQ testable configuration, we conduct a series of NOR-NOR PLA simulations. We use TSMC 0.6 μm SPDM technology to implement the PLA shown in figure 1. Figure 3(*a*) and figure 3(*b*) respectively show the full HSPICE simulation waveforms in the normal mode and the test mode of a fault-free PLA. When a resistive path (50 kΩ) exists between source and drain of PMOS1, we can find the fault by the HSPICE's Monte Carlo simulation with 30 sweeps by observing the larger power consumption in the presence of test vector 1. In contrast, if there is a short between source and drain of NMOS1, the fault will be located by vector 2 as well.

According to the above results of the HSPICE simulation, the ratio of the current introduced by the faulty circuits to that of the fault-free circuit is almost 5×10^5, as shown in table 2, which will be easily detected. Hence, the proposed transformation method indeed makes the IDDQ testing easily implemented in the PLAs to detect both bridge faults and open faults.

4. Conclusion

The proposed PLA configurations, adding one NMOS transistor in every product line and output line, can make PLAs IDDQ testable in the test mode. In these configurations, the controllability of every node is excellent for full IDDQ testability of PLAs. Then the IDDQ testing of PLA is just as simple as that of inverters with the benefits of low overhead, and only two vectors are required to proceed with testing. These IDDQ tests can be tested together with the general stand-by-current tests to achieve the goal of high quality control of CMOS ICs.

Acknowledgments

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